PLECS Model Quick Start Guide for Vienna PFC

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PLECS MODEL QUICK START GUIDE FOR VIENNA PFC

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXXXXA", where "XXXXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the PLECS Model Quick Start Guide for Vienna PFC . Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Website
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the Vienna PFC PLECS as a development tool. The manual layout is as follows:

- **"Introduction"**
- **Chapter 1. "PLECS Standalone Installation"**
- **Chapter 2. "Folder Structure"**
- **Chapter 3. "PLECS Settings"**
- **Chapter 4. "Starting a Simulation"**
- **Chapter 5. "Model Configurations"**
- **Chapter 6. "Modifying Control Parameters and Component Values"**
- **Chapter 7. "Monitoring Signals"**
- **Chapter 8. "Saving and Exporting Scope Traces"**
- **Chapter 9. "Power Meter"**

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

<table>
<tr><th>Description</th><th>Represents</th><th>Examples</th></tr>
<tr><td colspan="3">Arial font:</td></tr>
<tr><td rowspan="2">Italic characters</td><td>Referenced books</td><td>MPLAB® IDE User’s Guide</td></tr>
<tr><td>Emphasized text</td><td>...is the only compiler...</td></tr>
<tr><td rowspan="3">Initial caps</td><td>A window</td><td>the Output window</td></tr>
<tr><td>A dialog</td><td>the Settings dialog</td></tr>
<tr><td>A menu selection</td><td>select Enable Programmer</td></tr>
<tr><td>Quotes</td><td>A field name in a window or dialog</td><td>“Save project before build”</td></tr>
<tr><td>Underlined, italic text with right angle bracket</td><td>A menu path</td><td><u>File>Save</u></td></tr>
<tr><td rowspan="2">Bold characters</td><td>A dialog button</td><td>Click OK</td></tr>
<tr><td>A tab</td><td>Click the Power tab</td></tr>
<tr><td>N‘Rnnnn</td><td>A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.</td><td>4‘b0010, 2‘hF1</td></tr>
<tr><td>Text in angle brackets < ></td><td>A key on the keyboard</td><td>Press <Enter>, <F1></td></tr>
<tr><td colspan="3">Courier New font:</td></tr>
<tr><td rowspan="7">Plain Courier New</td><td>Sample source code</td><td>#define START</td></tr>
<tr><td>Filenames</td><td>autoexec.bat</td></tr>
<tr><td>File paths</td><td>c:\mcc18\h</td></tr>
<tr><td>Keywords</td><td>_asm, _endasm, static</td></tr>
<tr><td>Command-line options</td><td>-Opa+, -Opa-</td></tr>
<tr><td>Bit values</td><td>0, 1</td></tr>
<tr><td>Constants</td><td>0xFF, ‘A’</td></tr>
<tr><td>Italic Courier New</td><td>A variable argument</td><td>file.o, where file can be any valid filename</td></tr>
<tr><td>Square brackets [ ]</td><td>Optional arguments</td><td>mcc18 [options] file [options]</td></tr>
<tr><td>Curly brackets and pipe character: { | }</td><td>Choice of mutually exclusive arguments; an OR selection</td><td>errorlevel {0|1}</td></tr>
<tr><td rowspan="2">Ellipses...</td><td>Replaces repeated text</td><td>var_name [, var_name...]</td></tr>
<tr><td>Represents code supplied by user</td><td>void main (void)
{ ...
}</td></tr>
</table>

RECOMMENDED READING

This quick start guide describes how to use the Vienna PFC PLECS. Another useful document is listed below. The following Microchip document is available and recommended as a supplemental reference resource:

- **MSCICPFC/REF5 User's Guide - "*MSCSICPFC/REF5 3-Phase 30 kW Vienna PFC Reference Design*" (DS50002952**)

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (May 2020)

- Initial release of this document.

PLECS MODEL QUICK START GUIDE FOR VIENNA PFC

Introduction

INTRODUCTION

This document describes the procedure for installing PLECS simulation software, configuring the simulation settings, simulating the Vienna Power Factor Correction (PFC) model, and tutorial for using PLECS features used in the Vienna PFC model.

PLECS (Piecewise-Linear Electrical Circuit Simulation) is a simulation tool for power electronics circuits and systems. Using ideal switches, it simulates the dynamic behavior of complex systems quickly and efficiently. It uses a multi-domain approach to simultaneously simulate the control, electrical, magnetic, thermal, and mechanical domains. The Vienna PFC model incorporates the control, electrical, magnetic, and thermal domains to provide an accurate representation of the Vienna PFC Reference Design.

The design files, user's guide, and PLECS model of Microchip's 30 kW Vienna PFC Reference Design can be downloaded at the following link:

https://www.microchip.com/PFC

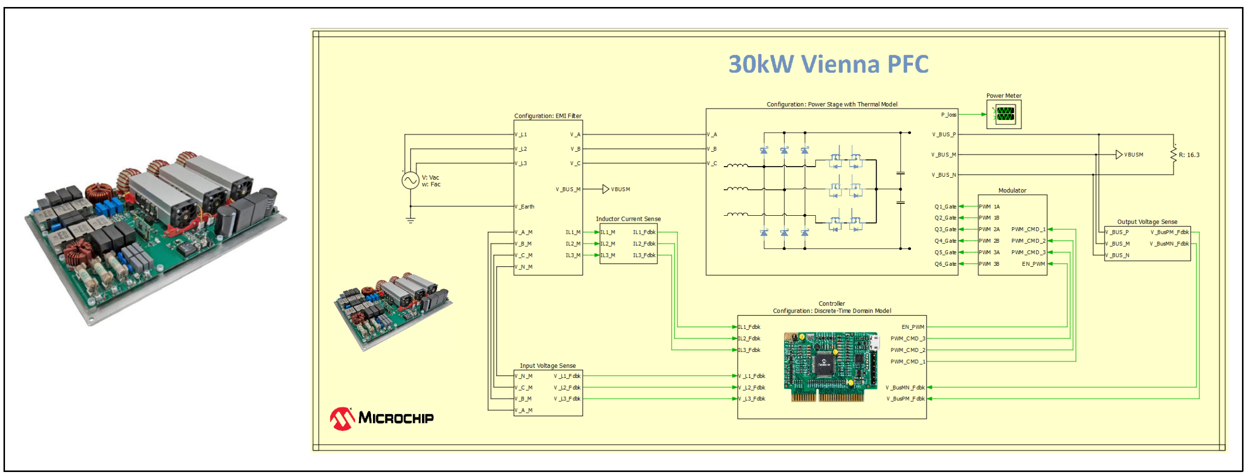

FIGURE 1: *Vienna PFC Reference Design and PLECS Model.*

Chapter 1. PLECS Standalone Installation

Plexim, the developer of PLECS, offers two versions of the software: PLECS Blockset and PLECS Standalone. PLECS Blockset operates within the Simulink environment, using Matlab as its processing engine. PLECS Standalone is a complete power electronics simulation platform with its own processing engine, which enables it to run much faster than PLECS Blockset. Both versions have identical core capabilities and models can be exchanged between the two versions.

The Vienna PFC Reference Design was modeled using PLECS Standalone. For a trial version of PLECS Standalone, follow the instructions at the Plexim link at the end of this section to download, install, and request trial license. Without a license, PLECS Standalone operates in demo mode, allowing users to build and simulate models. However, the models cannot be saved, and the session is time-limited to 60 minutes.

During the installation process, change the default destination folder path to C:\Plexim\PLECS 4.x (64 bit), as shown in Figure 1-1.

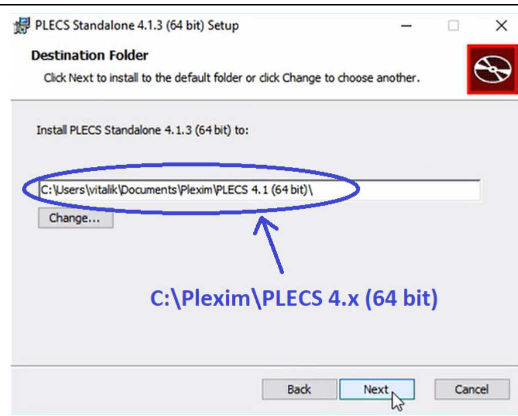

FIGURE 1-1: *Changing the Destination Folder Path in the Setup Wizard.*

When requesting a license, select the 'PLECs PIL' checkbox to include Processor-In-the-Loop capability, as illustrated in Figure 1-2.

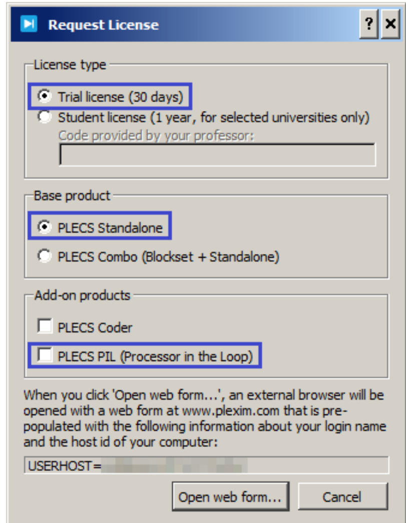

FIGURE 1-2: *Requesting Standalone Trial License.*

For a video walk-through of the PLECS Standalone installation, see:

- Windows: https://www.plexim.com/support/videos/installing-standalone-win
- Mac: https://www.plexim.com/support/videos/installing-standalone-mac

Chapter 2. Folder Structure

Extract the provided Vienna PFC model zip file to: C:\Plexim.

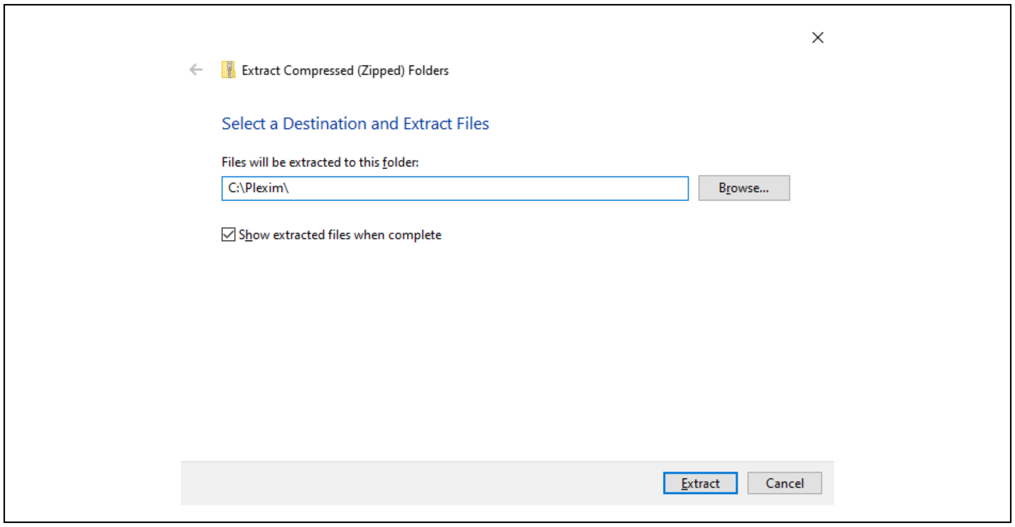

FIGURE 2-1: *Extracting Compressed Folders.*

The zip file contains two folders: Projects and Component Models. The Projects folder contains a subfolder for the Vienna PFC reference design. Future reference designs will be added to this folder. Within the Vienna-PFC folder are subfolders containing support files, including source code for running Processor-In-the-Loop. The Component Models folder contains the thermal descriptions for the Microchip SiC Schottky barrier diode and SiC MOSFET used in the Vienna PFC reference design.

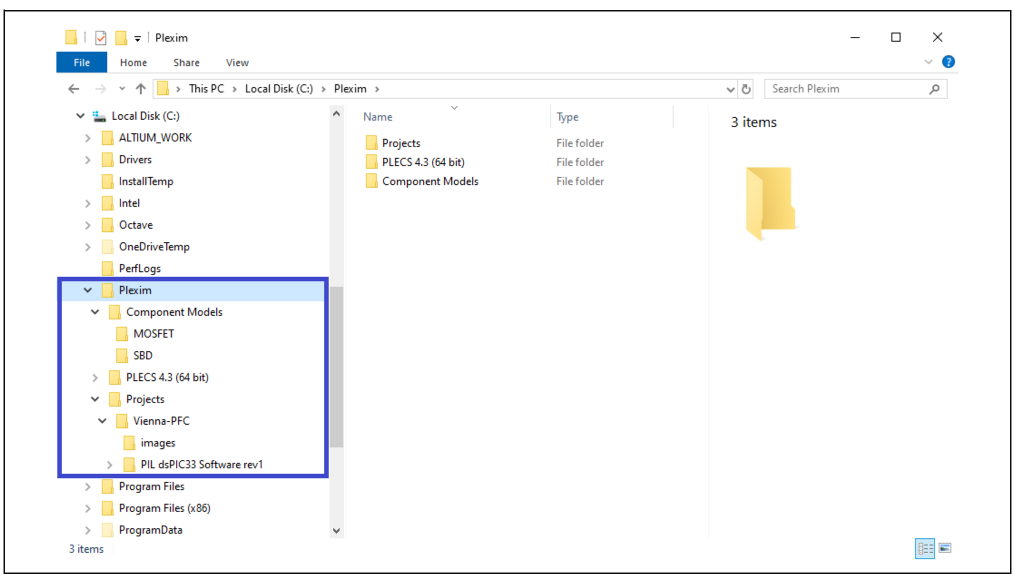

FIGURE 2-2: *Folder Structure.*

Chapter 3. PLECS Settings

Double-click on the model file, Vienna-PFC rev1.plecs, which is found within the Vienna-PFC project folder. The model and library browser will open.

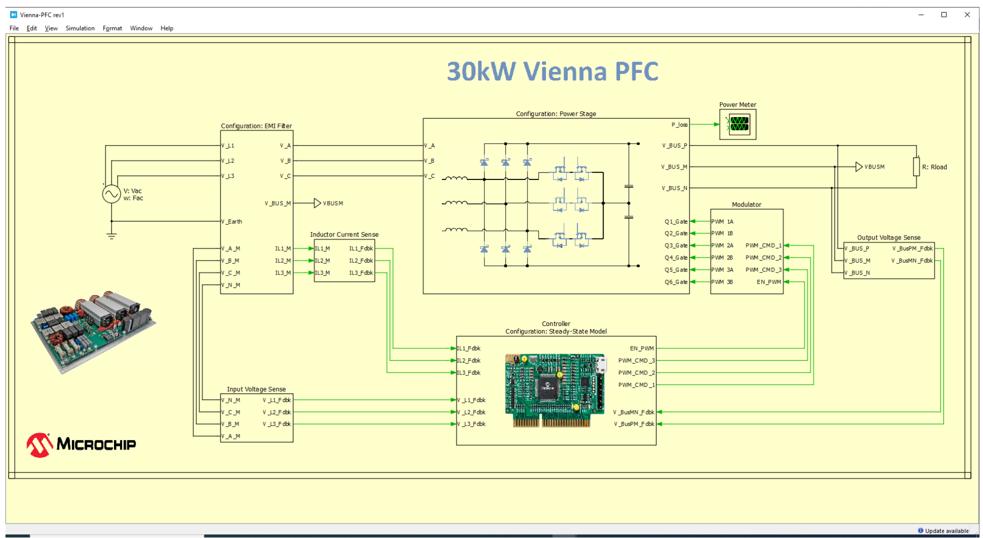

FIGURE 3-1: *Vienna PFC Top-Level. Model.*

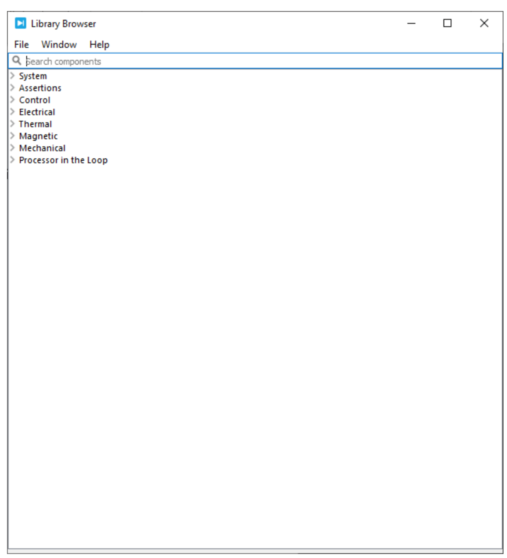

FIGURE 3-2: *Library Browser.*

If the PIL add-on license is not available, the following warning will appear when the model is opened. Click OK and continue. Instructions on how to obtain a PIL trial license are shown in the PLECS installation section.

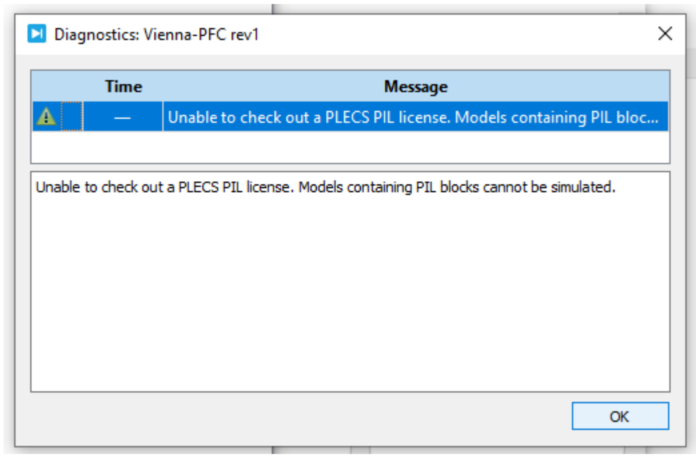

FIGURE 3-3: *PIL License Warning.*

Under File/PLECS Preferences in the General tab, increase the cache size limit preferably to 4 GBytes but no more than one-third of the physical memory of the computer. The user may adjust other preferences such as DIN or ANSI schematic symbol.

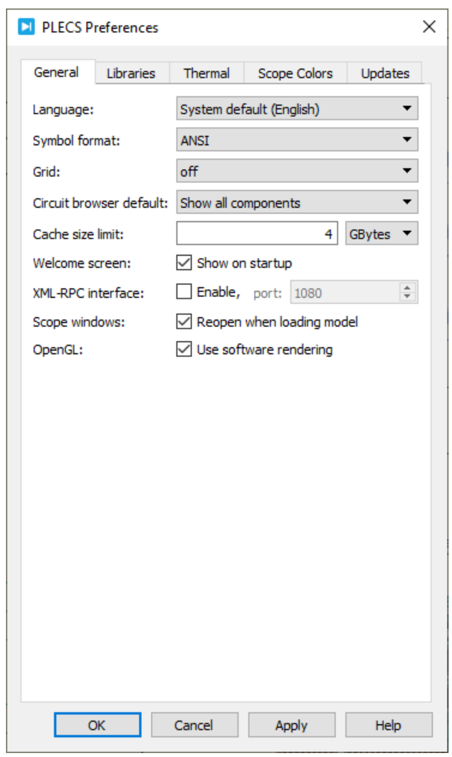

FIGURE 3-4: *PLECS Preferences.*

Next, under the Thermal tab, add the path to the MOSFET and SBD (Schottky barrier diode) folders containing the thermal descriptions.

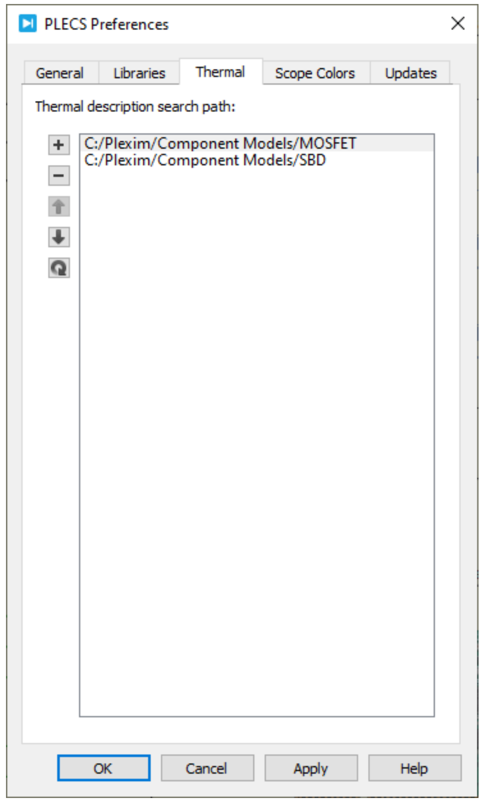

FIGURE 3-5: *Adding Paths to the Thermal Descriptions.*

Chapter 4. Starting a Simulation

To run the model, select Simulation / Start or press CTRL+T. This will run the default configuration of a 10-second simulation time, 230 V_{RMS} line voltage (corresponding to a 400 V_{RMS} three-phase voltage), 50 Hz line frequency, and 7.5 kW load. To adjust these settings, select Simulation/Simulation parameters or press Ctrl+E. In the Solver tab, adjust the highlighted field below for the desired stop time.

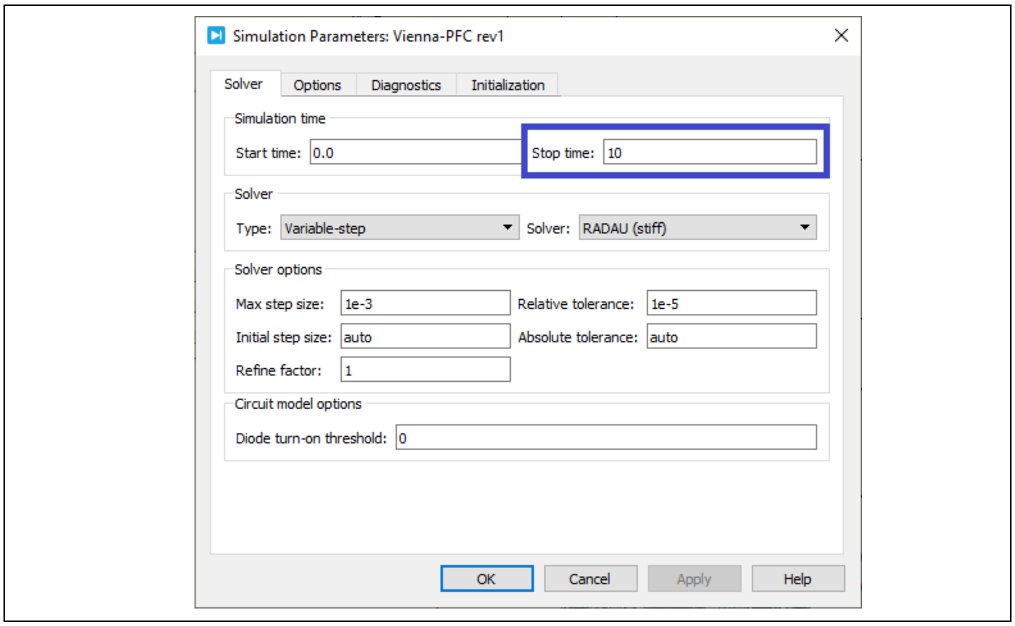

FIGURE 4-1: *Simulation Parameter Vienna Stop Time.*

To adjust the line and load settings, select the Initialization tab. The commands listed in this window below are run once at the start of simulation. The syntax used to define the variables is the same used in a Matlab or Octave script.

In PLECS, all component values are purely numerical without any units specified. Volts is used for voltage, Hertz for frequency, and Ohms for resistance. Matlab e-notation (scientific notation) can be used to define values. For example, a 10kΩ resistor can be set to `10000` or `10e3`. The variable for the load resistor, R_{load}, is set to:

EQUATION 4-1:

$$R_{load} = \frac{(700\,V)^2}{7.5\,kW}$$

Entered into PLECS as:

```
Rload = 700^2/7.5e3;
```

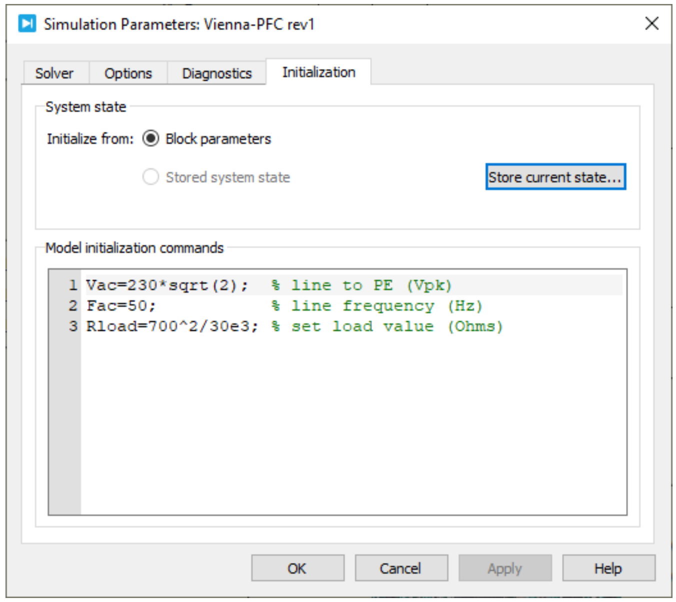

FIGURE 4-2: *Model Initialization.*

The three-phase voltage source component used in the model accepts parameters: Amplitude, Frequency, and Phase offset. As shown below, the variables defined in the initialization are passed to the voltage source. This approach allows the line conditions to be available to the other model blocks. The phase offset can be set to any value. The default value shown below was selected to reduce simulation time as the PFC is not enabled until after a zero-cross is detected.

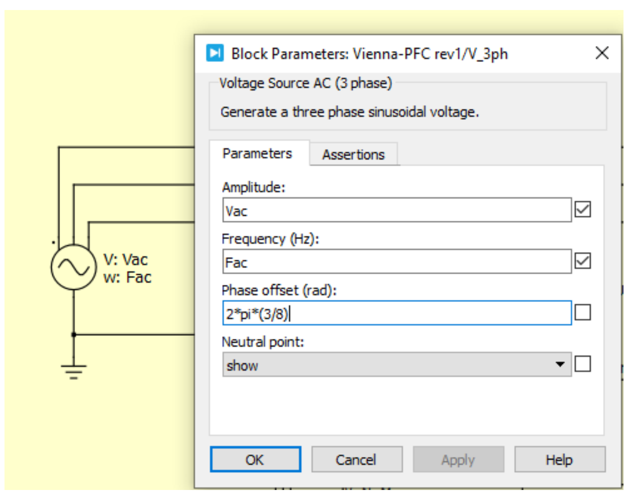

FIGURE 4-3: *Voltage Source Parameters.*

Chapter 5. Model Configurations

PLECS allows a model block to be associated with multiple schematics or configurations. In PLECS, blocks are referred to as subsystems and subsystems with multiple configurations are referred to as configurable subsystems. Configurable subsystems are used for the Front-End Input, Power Stage, and Controller stages. The model is setup with the EMI Filter, Power Stage with Thermal Model, and Steady-State Model configurations as the default.

5.1 FRONT-END INPUT

The front-end input default configuration is an EMI filter. This contains the passive elements of the filter as well as voltage and current sensing points. Alternatively, to reduce the simulation time by nearly 30%, the user may select Input Sense. The Input Sense configuration does not contain any passive elements, it only has voltage and current sensing points. Therefore, using the Input Sense configuration does not result in accurate electrical and thermal losses as compared to the EMI filter. However, it does allow one to evaluate the controller behavior or have a reasonable estimate of the switch losses.

Double-click the block highlighted below to select between configurations.

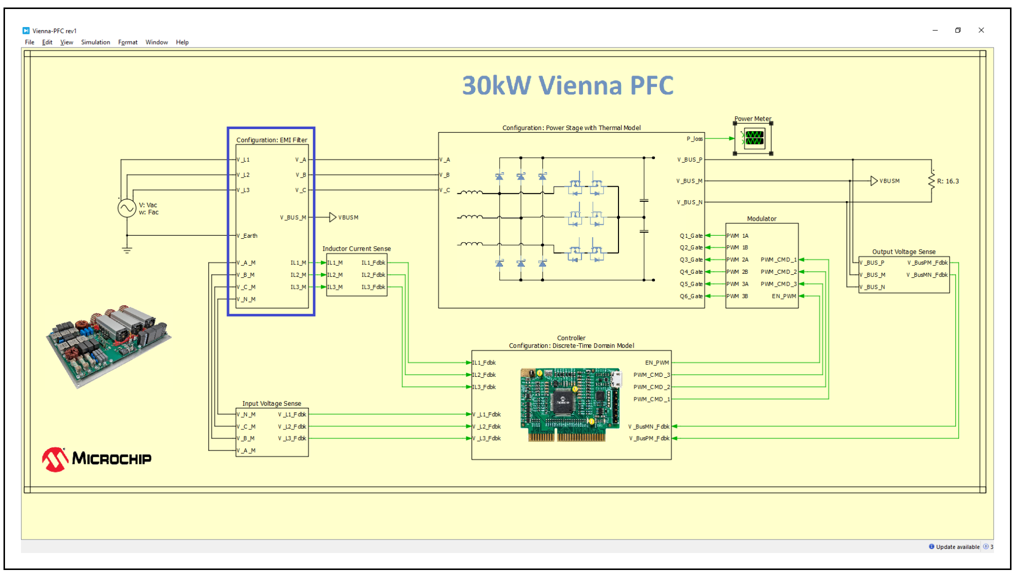

FIGURE 5-1: *Front-End Input.*

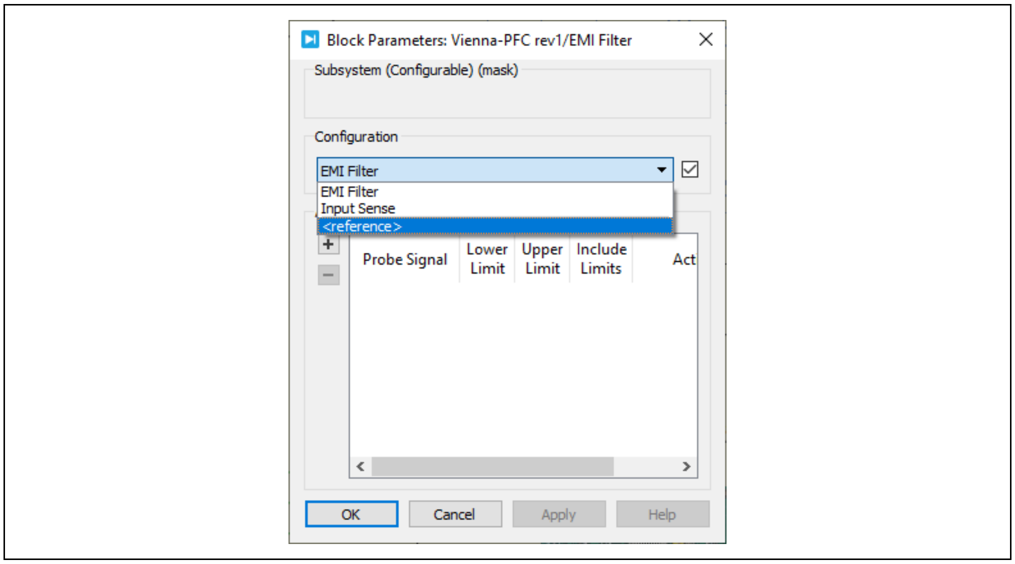

FIGURE 5-2: *Front-End Input Subsystem Selection.*

5.2 POWER STAGE

The model contains two power stage configurations: Power Stage and Power Stage with Thermal Model. The thermal model includes:

- Boost inductor core loss
- Schottky barrier diode conduction loss and temperature
- MOSFET conduction loss, switching loss, and temperature
- Heat sink temperature

Since the thermal model considerably increases simulation time, a configuration without the thermal model is included.

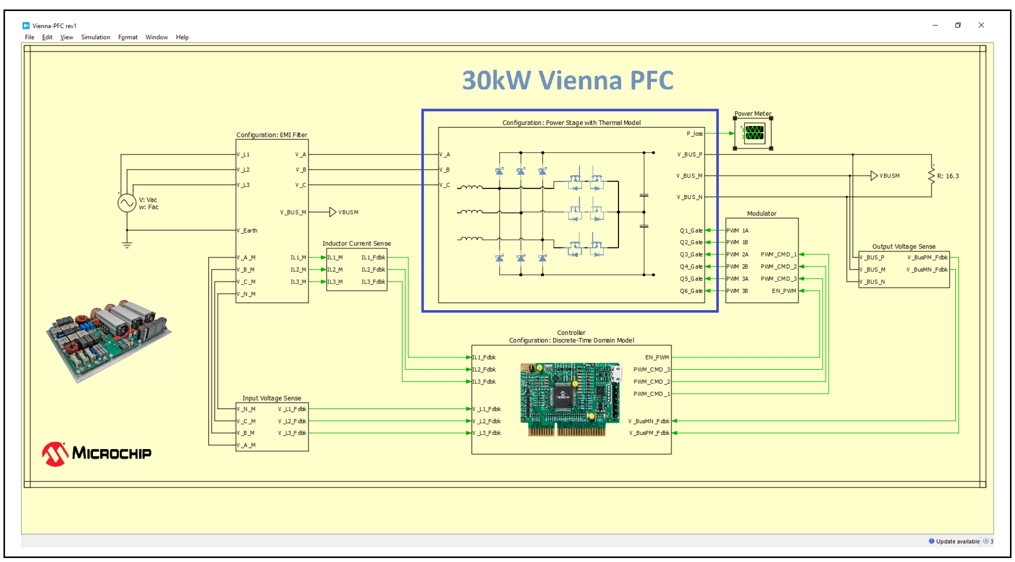

FIGURE 5-3: *Power Stage.*

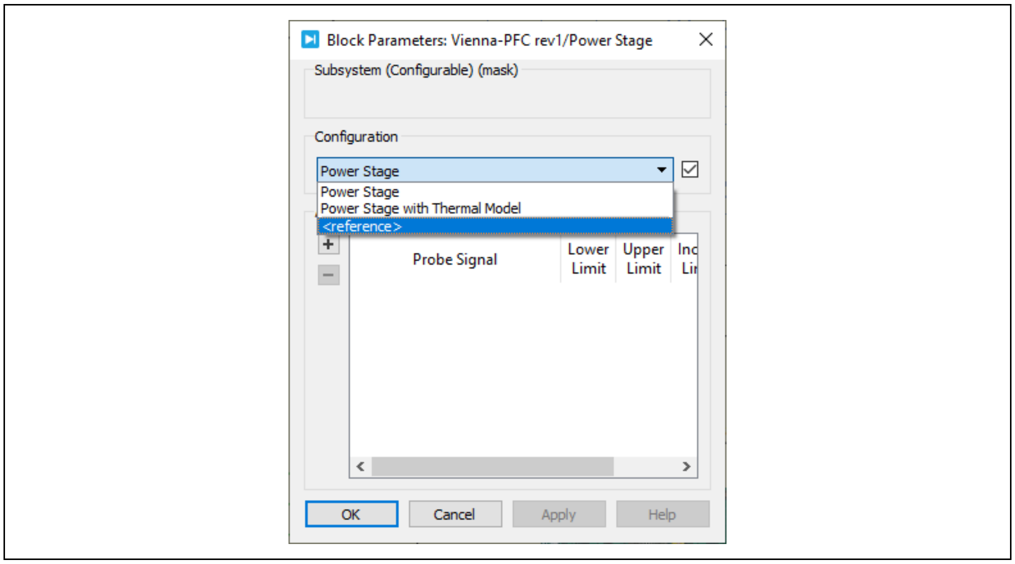

FIGURE 5-4: *Power Stage Subsystem Selection.*

5.3 CONTROLLER

The model contains three controller configurations: Steady-State Model, Discrete-Time Domain Model, and Processor-In-the-Loop. The Steady-State Model configuration provides quick startup and transient response in order to reach a steady state without running through soft-start at startup or be slowed down by the PI controllers during transient events. This is useful for thermal and efficiency simulations. Additionally, this configuration operates in the continuous-time domain.

The Discrete-Time Domain Model configuration operates at an update rate of 35 kHz. The model includes all the controls features of the Vienna PFC reference design except for the in-rush relay control, protection, and diagnostics. The model's control behavior and timing are strongly correlated to that of the reference design. However, the simulation runs slower than the Steady-State Model configuration.

The Processor-In-the-Loop configuration allows the control algorithm to run on the dsPIC33CH512MP506 DP Plug-In Module (PIM) via a USB connection. This enables development and debugging of the control algorithm on the target processor with the power stage and sensing simulation in PLECS. PIL software is provided with the Vienna PFC PLECS model package for flashing into the dsPIC DSC Master and Slave cores.

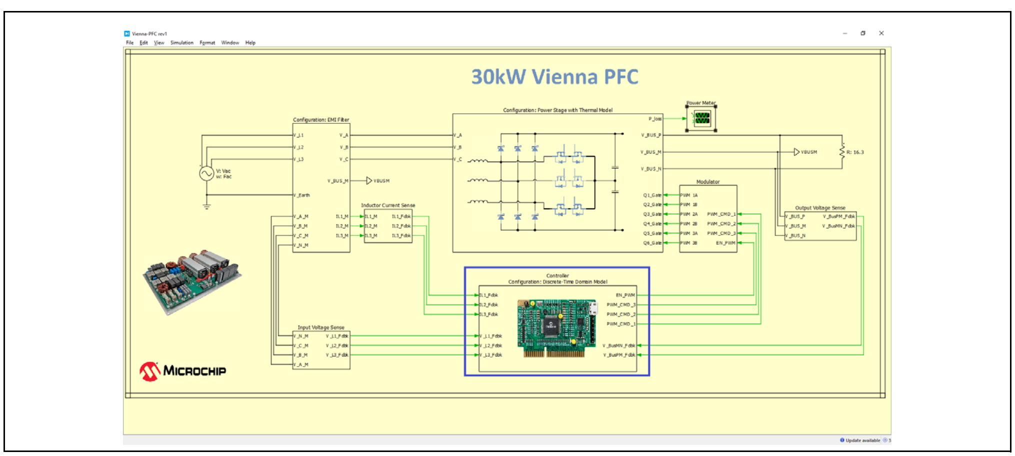

FIGURE 5-5: *Controller.*

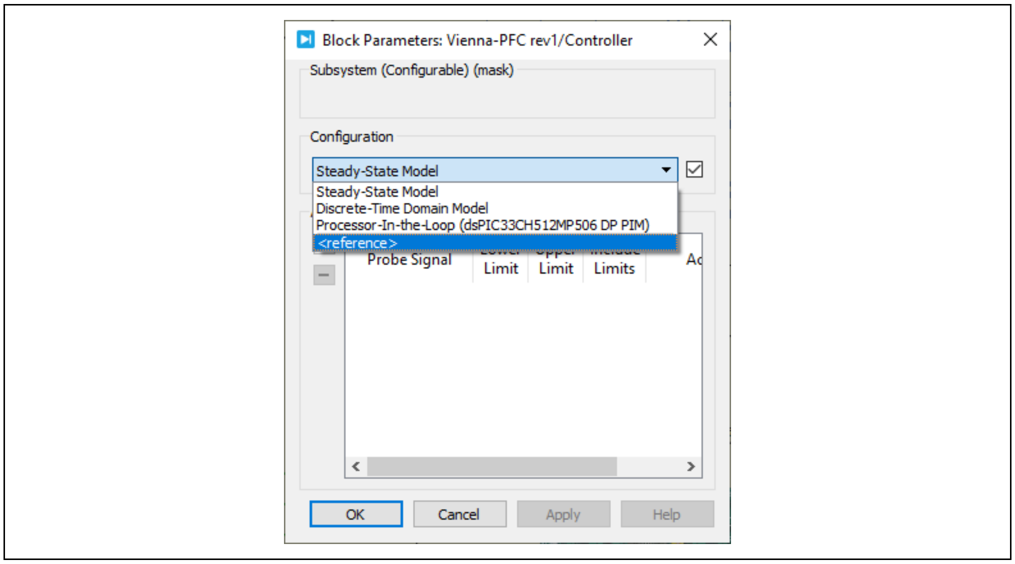

FIGURE 5-6: *Controller Subsystem Selection.*

Chapter 6. Modifying Control Parameters and Component Values

At the start of simulation, PLECS executes the initialization commands under the Simulation Parameters Initialization tab. The variables are available as global variables to components and subsystems. It also executes the initialization commands contained in the mask of each subsystem. Variables defined in a mask are local to the subsystem. These variables cannot be modified after the simulation starts.

To edit the mask, right-click the subsystem and select Edit mask as shown below or by Ctrl+M. Then, select the Initialization tab.

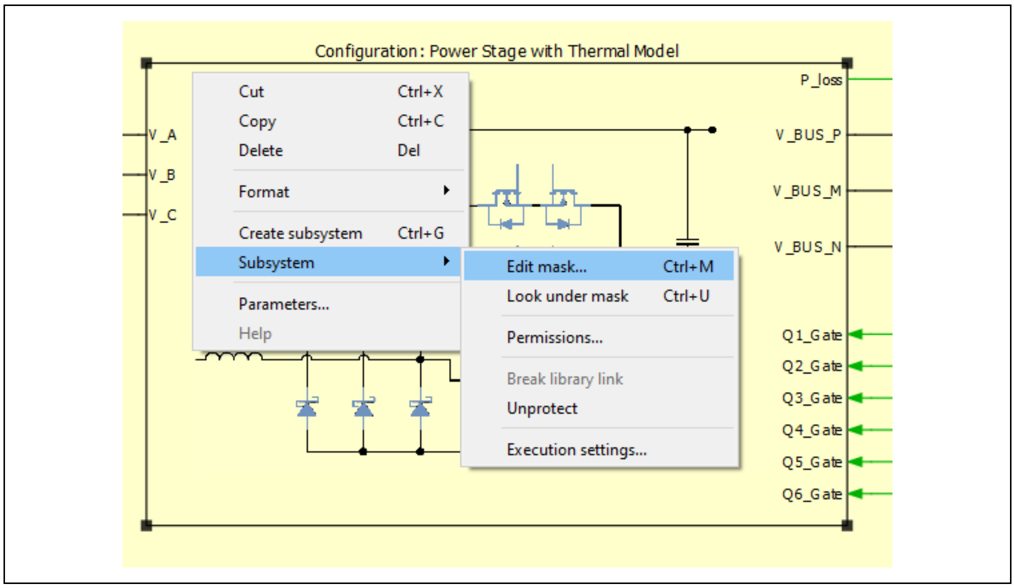

FIGURE 6-1: *Editing the Mask.*

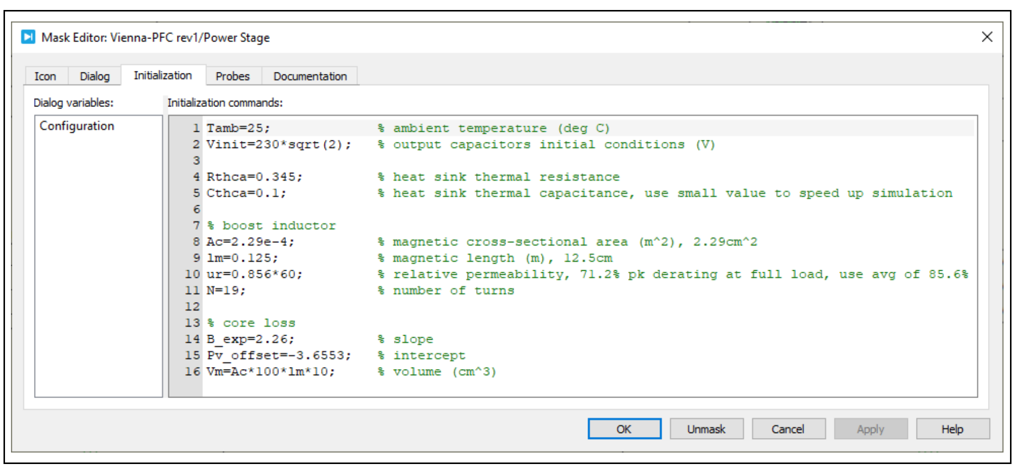

FIGURE 6-2: *Mask Editor.*

During simulation, values defined in components, such as voltage sources, resistors, or control components, can be modified. For example, the output load resistor, initially defined by variable `Rload` can be adjusted to `1.2*Rload` to increase the resistance by 20% or to `16.3` to set it to a 16.3Ω, corresponding to a 30 kW load. Double-click the component's value field and enter in the desired value.

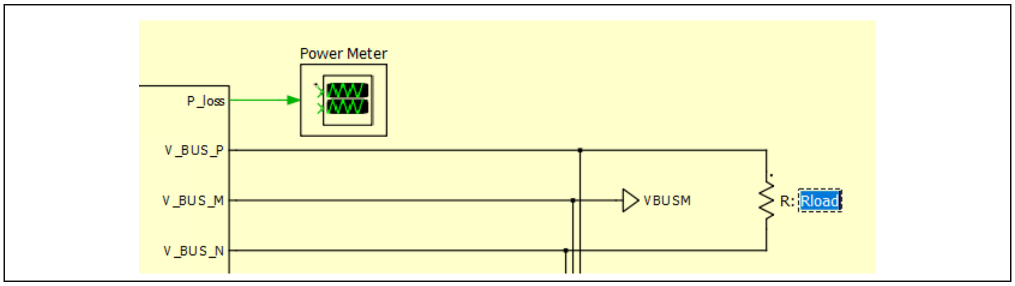

FIGURE 6-3: *Modifying a Component Value.*

To open a subsystem:

- Double-click the subsystem (not applicable to configurable subsystems)
- Right-click the subsystem, select Subsystem/Look under mask
- Select the subsystem with a single-click, followed by Ctrl+U

PLECS protects subsystems to prevent inadvertent modifications. To unprotect a subsystem, right-click the subsystem (Ctrl+U), select Subsystem/Unprotect.

Adjusting the gain block of a PI controller during simulation is easily done by opening the controller subsystem and double-click of the gain block. In the example, the controller's proportional gain is set to `Kpv`. It can be adjusted to any desired value to see the effect on the circuit.

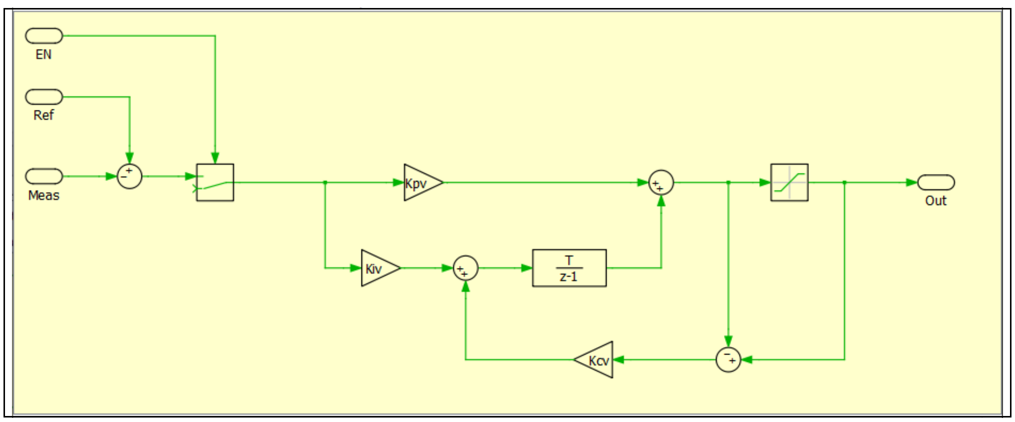

FIGURE 6-4: *PI Controller.*

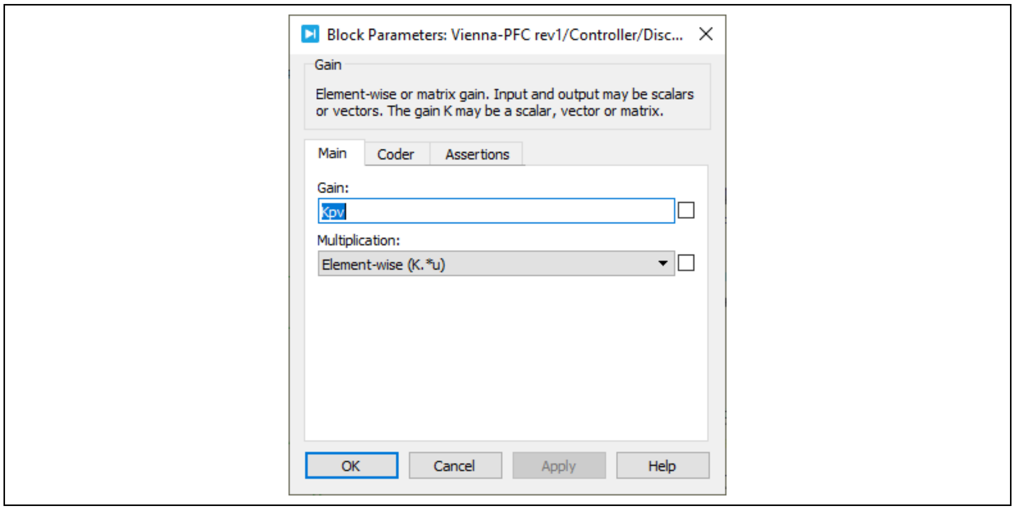

FIGURE 6-5: Block Parameters Vienna PFC.

PLECS includes switches that can be operated during the simulation. The following subsystem is the third-harmonic injection for balancing the voltage on the output capacitors. To disable this feature, the user may double-click the Manual Switch.

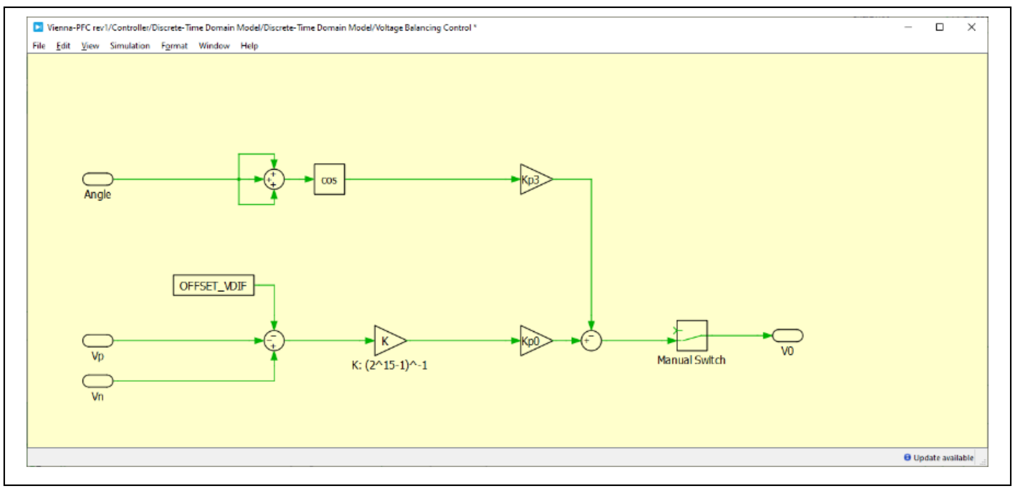

FIGURE 6-6: Manual Switch.

Chapter 7. Monitoring Signals

In PLECS, a scope or display may be used to monitor signals real-time while the simulation is running. Signals are only monitored in the control domain. Signals in the electrical, magnetic, thermal, or mechanical domain cannot be monitored directly. Instead, meters, such as voltmeter, MMF meter, thermometer, or torque sensor, are used to convert the signal from the respective domain to the control domain. An alternative to using meters is to use probes. Probes convert physical attributes of a component or subsystem to the control domain. Many components in PLECS have internal signals associated with them that a probe can monitor. Refer to a specific component's documentation to learn what probe signals it includes.

7.1 MULTI-DOMAIN MODEL

Domains are color-coded as shown in Figure 7-1.

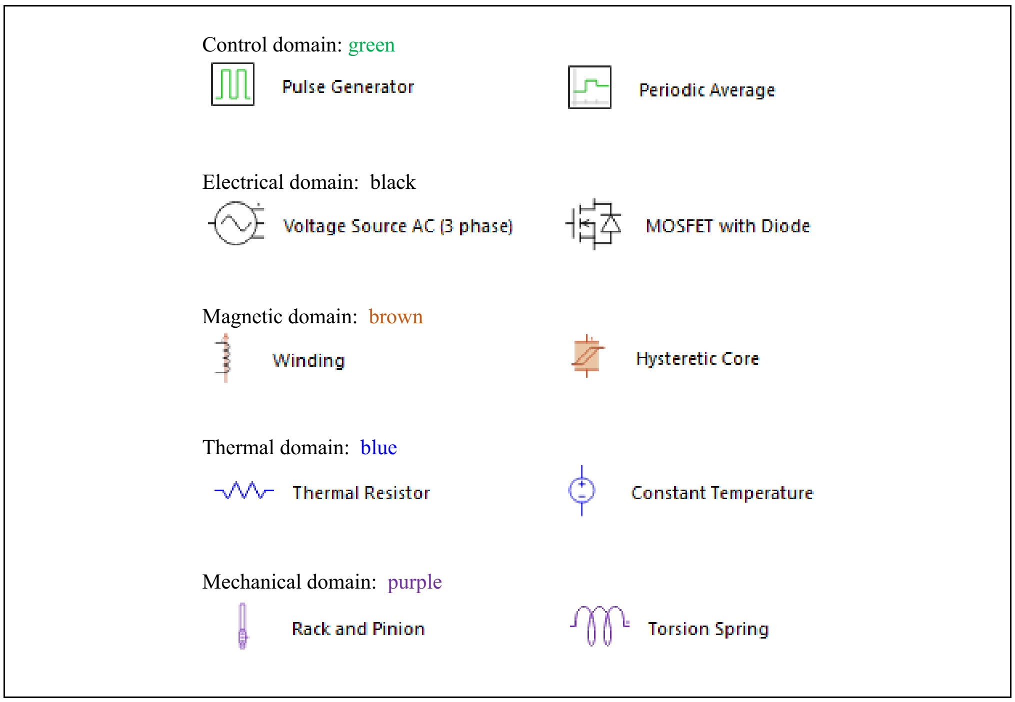

FIGURE 7-1: *Color-Coded Components for the Different Domains.*

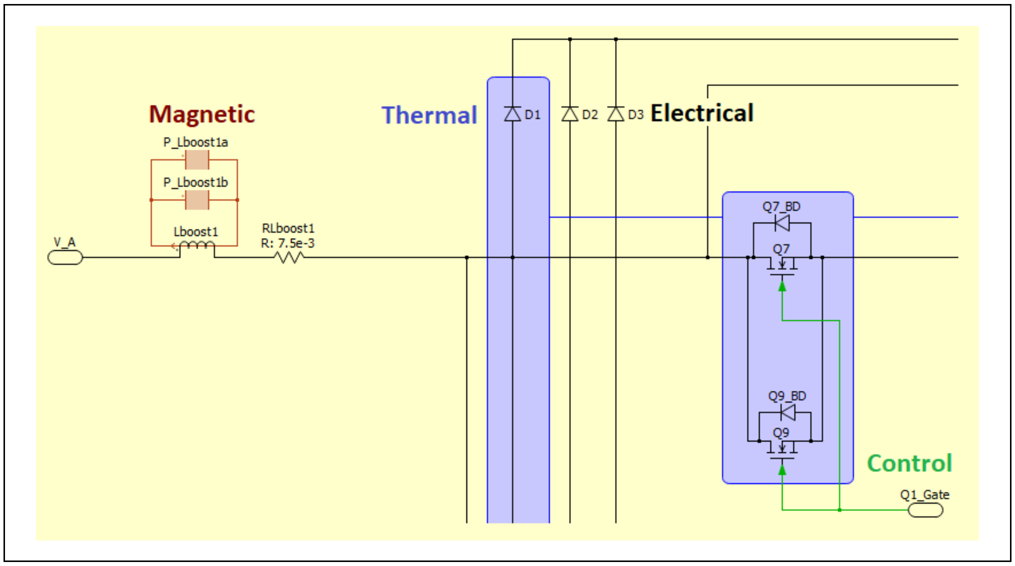

FIGURE 7-2: *A Multi-Domain Schematic Example.*

7.2 MONITORING A SIGNAL WITH A METER

To monitor the voltage across two nodes, for example, use a voltmeter from the library browser. The library browser automatically opens on PLECS start-up. It also be accessed by selecting Window/Library Browser from the menu or by Ctrl+L. Drag it from the library browser onto the schematic by clicking on the component and holding down the mouse button. Use Ctrl+R to rotate and Ctrl+F to flip the component. Once positioned onto the schematic, you can rename the meter, if desired. Next, connect the black terminals to the electrical nodes of the circuit.

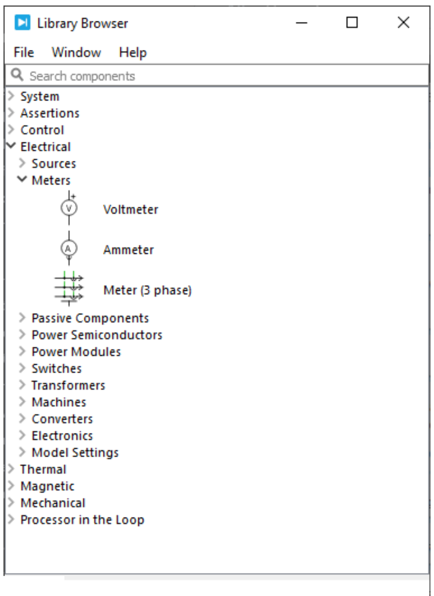

FIGURE 7-3: *Library Browser Electrical Meters.*

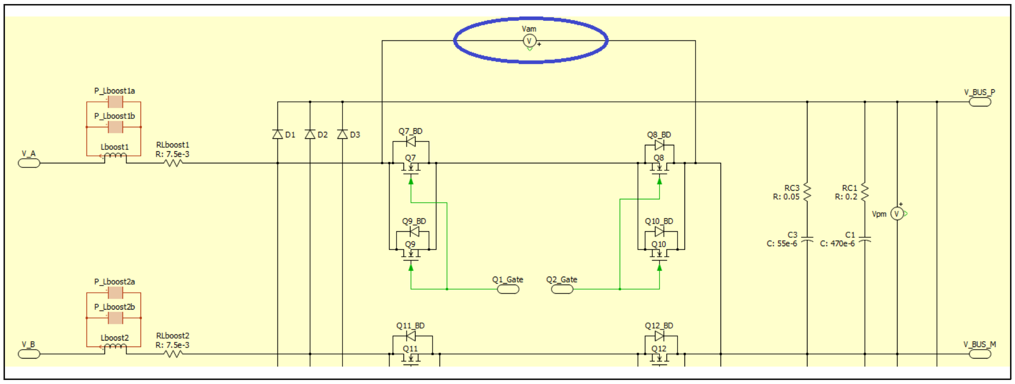

FIGURE 7-4: *Voltage Measurement using Voltmeter.*

Next, drag a *Scope* from the library browser to the schematic. You can find it under the System or type in scope in the search bar. Connect the green terminal of the *Voltmeter* to the *Scope*.

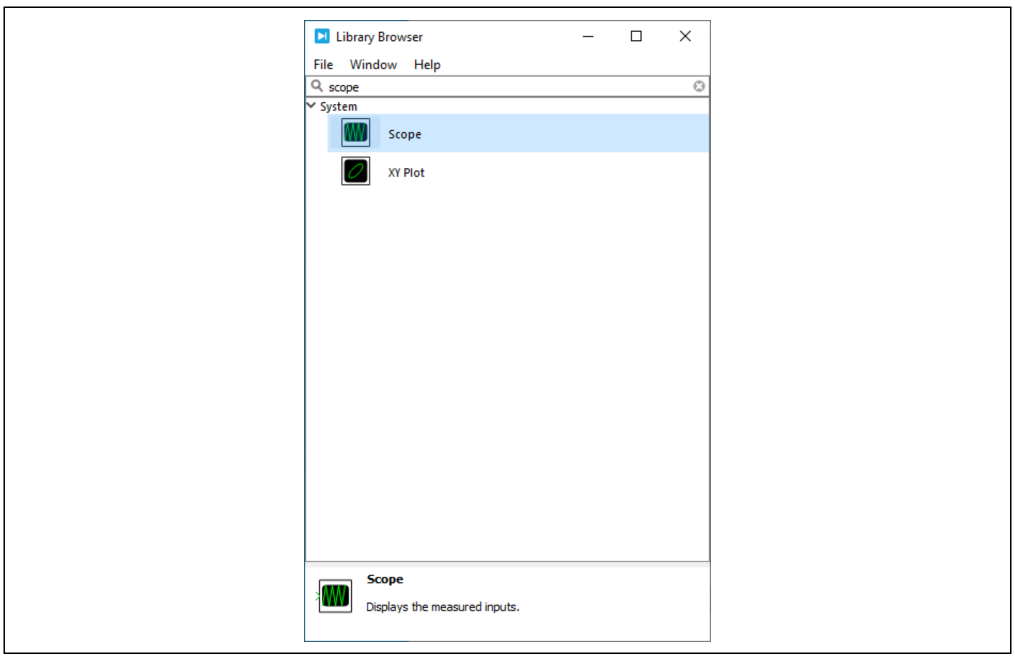

FIGURE 7-5: *Library Browser Scope.*

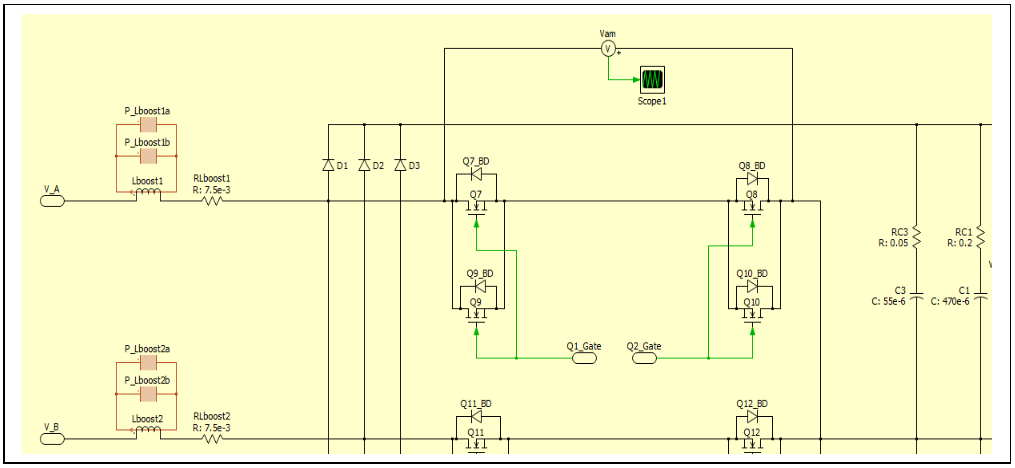

FIGURE 7-6: *Power Meter.*

Run the simulation (Simulation / Start or Ctrl+T). Double-click the scope to see the signal trace. To zoom in on the time-axis, click on the plot and drag the mouse horizontally. To zoom in on the voltage-axis, click and drag the mouse vertically.

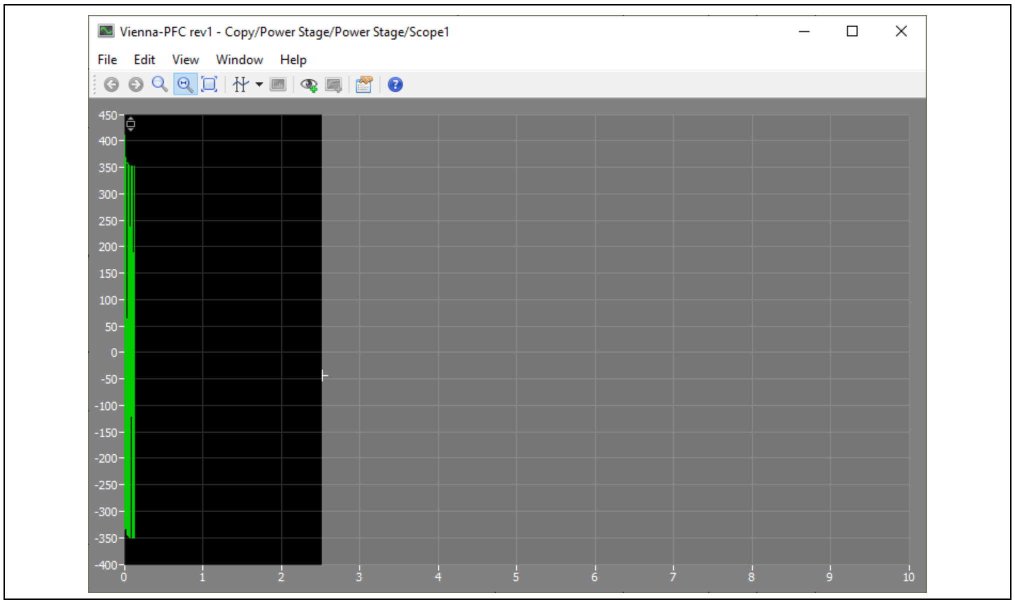

FIGURE 7-7: *Zooming on Time-Axis.*

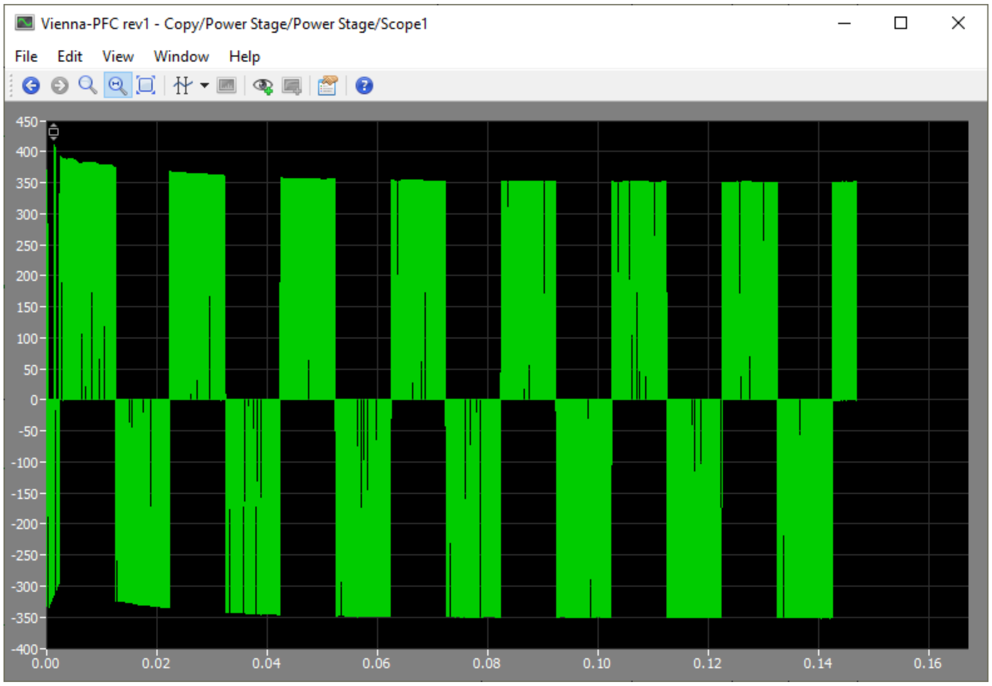

FIGURE 7-8: *Zoomed in Time-Axis.*

Measuring current is done is a similar way, except the Ammeter connects inline with the electrical signal:

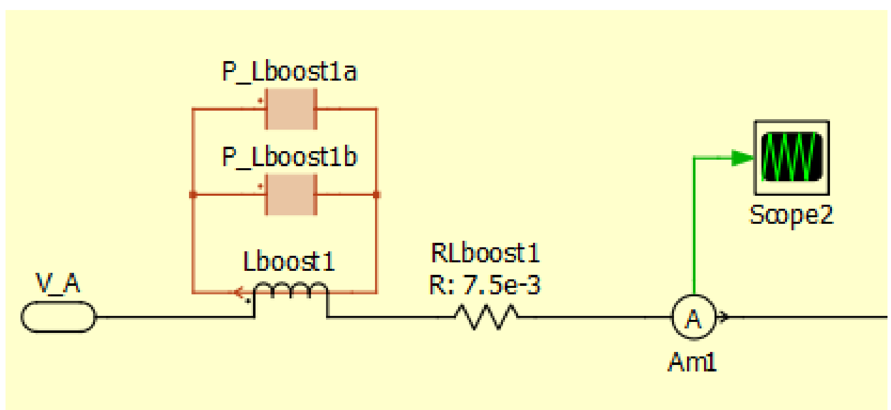

FIGURE 7-9: *Ammeter.*

7.3 MONITORING SIGNALS ON MULTIPLE PLOTS

Scopes can have multiple plots by adjusting the number of plots in the Scope Parameters window. The scope will have a green terminal for each plot:

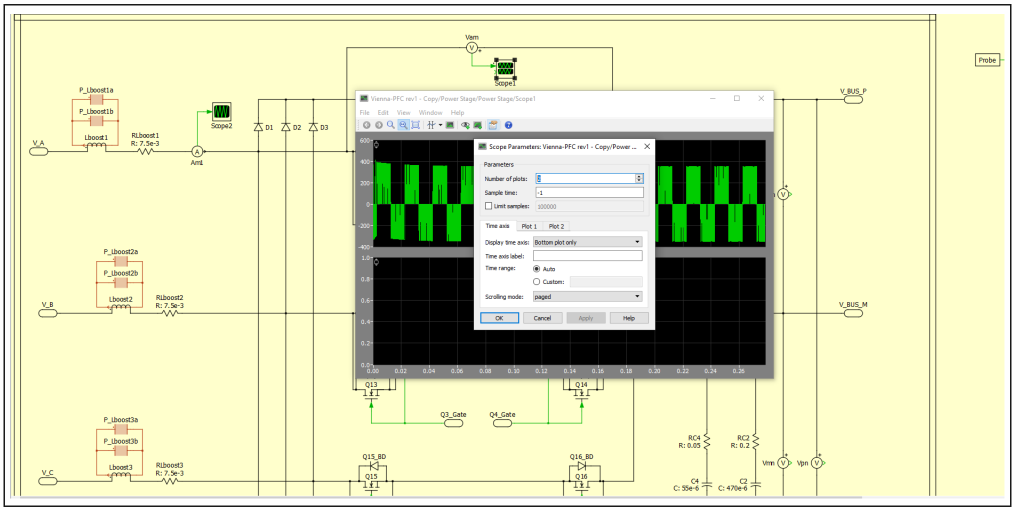

FIGURE 7-10: Multiple Plot Selection.

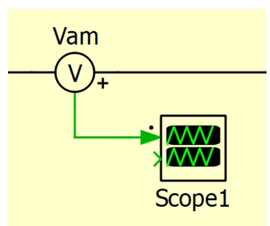

FIGURE 7-11: Multi-Plot Scope.

The example below monitors the switched-node voltage with respect to the mid-point of the DC bus in the top plot. The bottom plot monitors the boost inductor current.

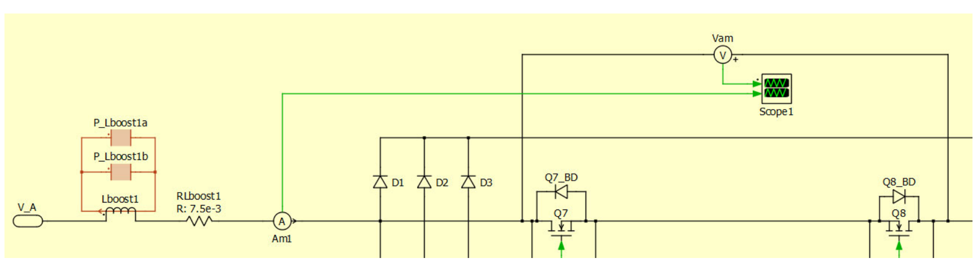

FIGURE 7-12: Scope Monitoring Voltage and Current.

7.4 MONITORING SIGNALS ON A SINGLE PLOT

Multiple signals can be multiplexed together using a Signal Multiplexer:

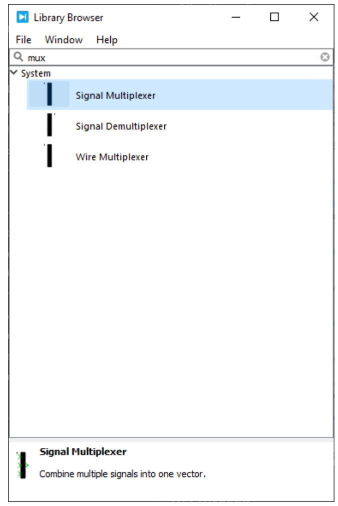

FIGURE 7-13: *Signal Multiplexer.*

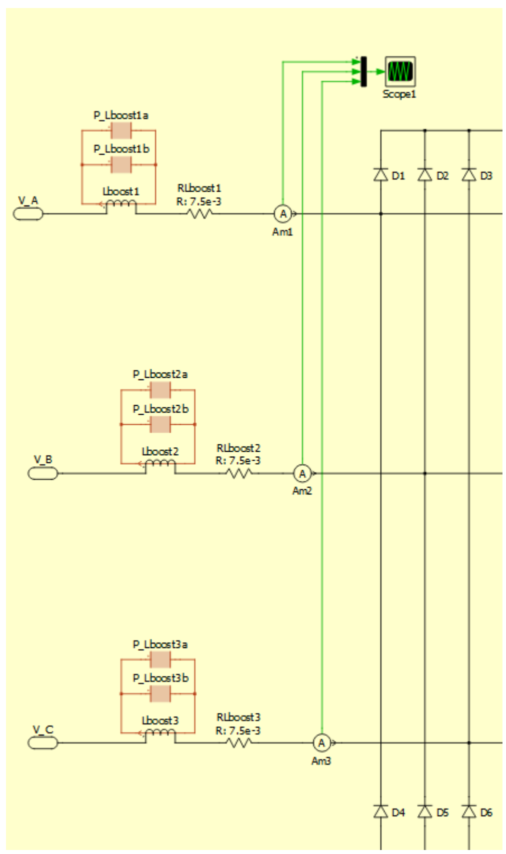

FIGURE 7-14: *Signals Multiplexed to a Scope.*

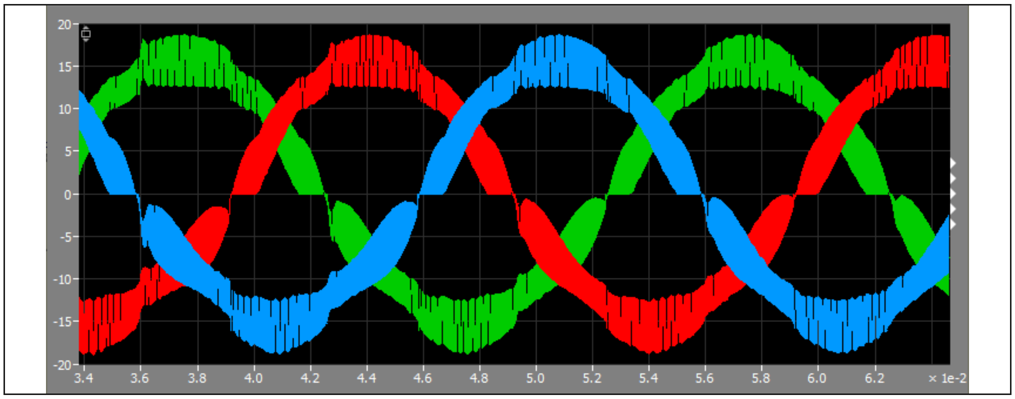

FIGURE 7-15: *Multiple Signals on Single Scope Plot.*

7.5 MONITORING COMPONENT SIGNALS WITH PROBE

Components and some subsystems have signals available that do not require access through a meter. Instead, it is accessible with the Probe component found in the library browser. Place the Probe on the schematic and double-click. Next, select and drag a component from the schematic onto the Probe window.

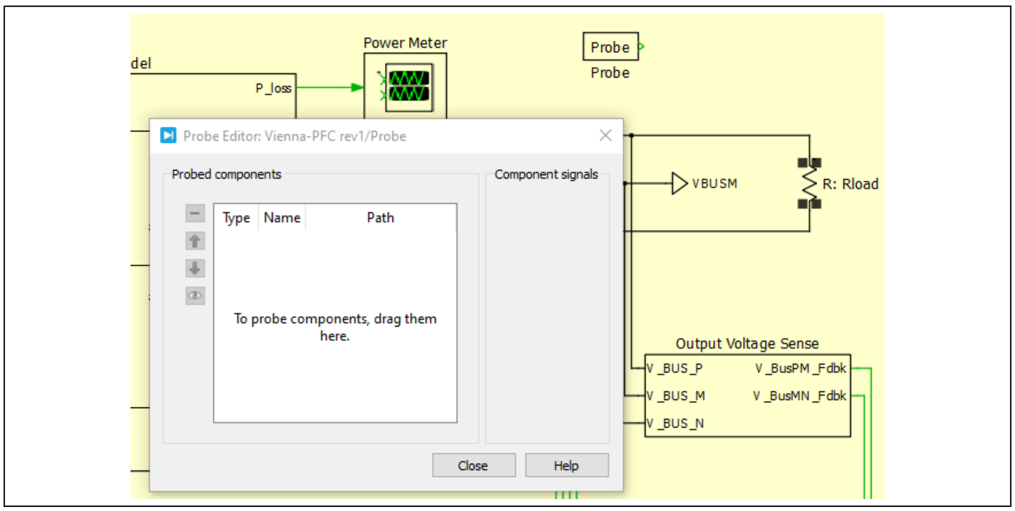

FIGURE 7-16: *Probe Dialog Window.*

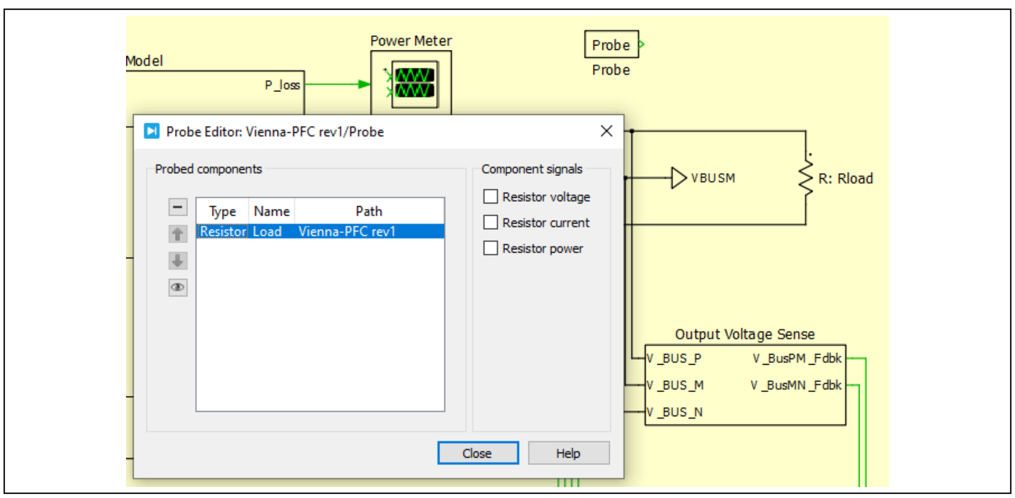

FIGURE 7-17: *Available Component Signals in Probe Dialog Window.*

Attributes of the component appear in the Probe window. Select the desired signal. Connect a Scope to the Probe and start the simulation (Ctrl+T).

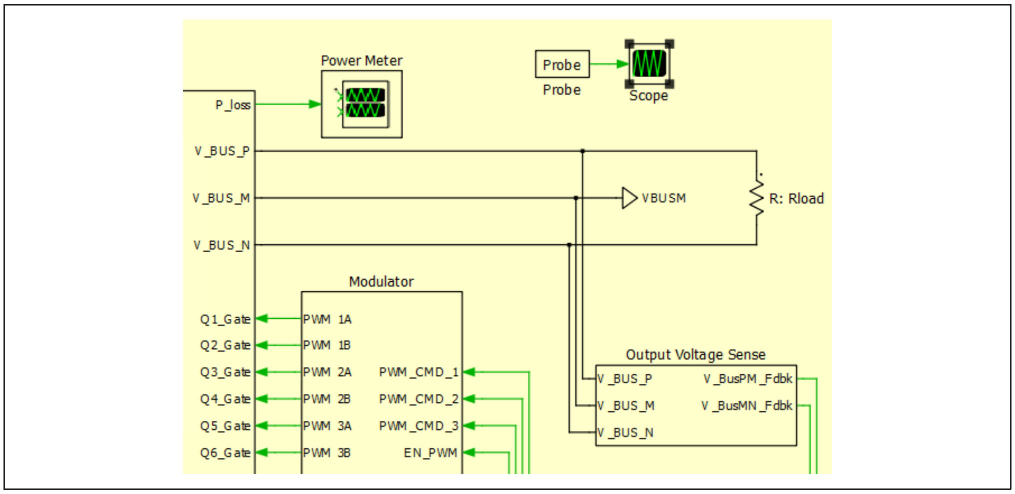

FIGURE 7-18: *Probe Connection to Scope.*

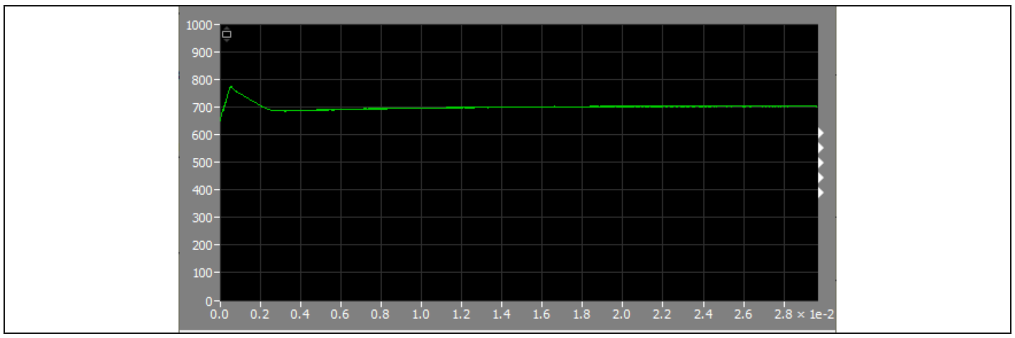

FIGURE 7-19: *Probe Signal Plotted in Scope.*

7.6 MONITORING SUBSYSTEM SIGNALS WITH PROBE

To simplify the measurement of various circuits and subsystems, the Vienna PFC model includes predefined probes within the power stage and controller schematics. Additionally, the top-level subsystems have signals available that only require a probe and scope. For example, the PWM input and output signals of the Modulator are accessible by dragging the Modulator onto a Probe window.

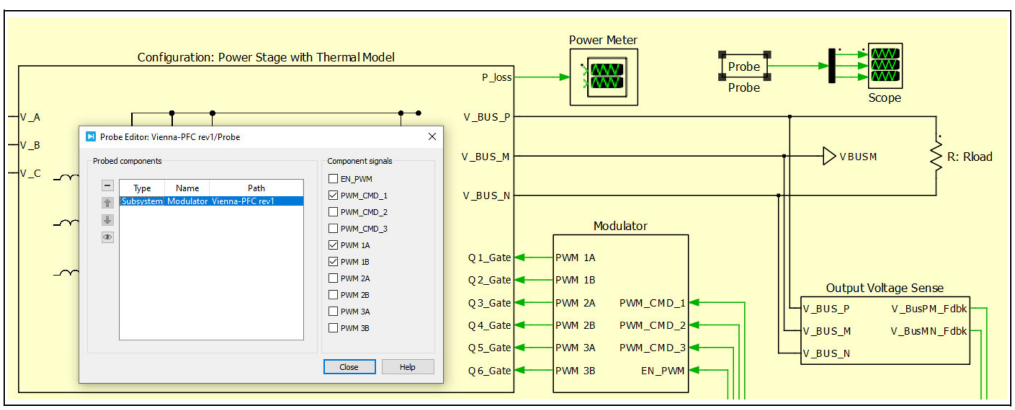

FIGURE 7-20: *Available Subsystem Signals in Probe Dialog Window.*

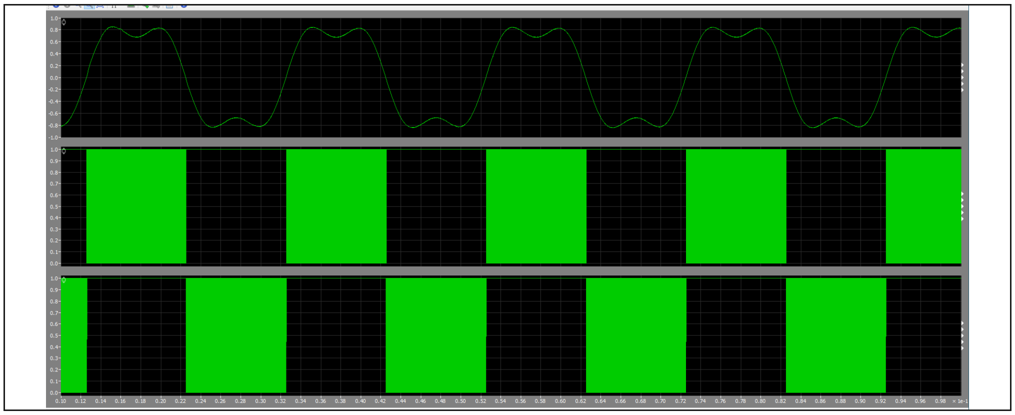

FIGURE 7-21: Probe Signals Plotted in Scope.

Chapter 8. Saving and Exporting Scope Traces

Data plot in a Scope can be saved to a PLECS *.trace file by selecting File/Save trace data. It can be loaded in subsequent simulation runs using File/Load trace data.

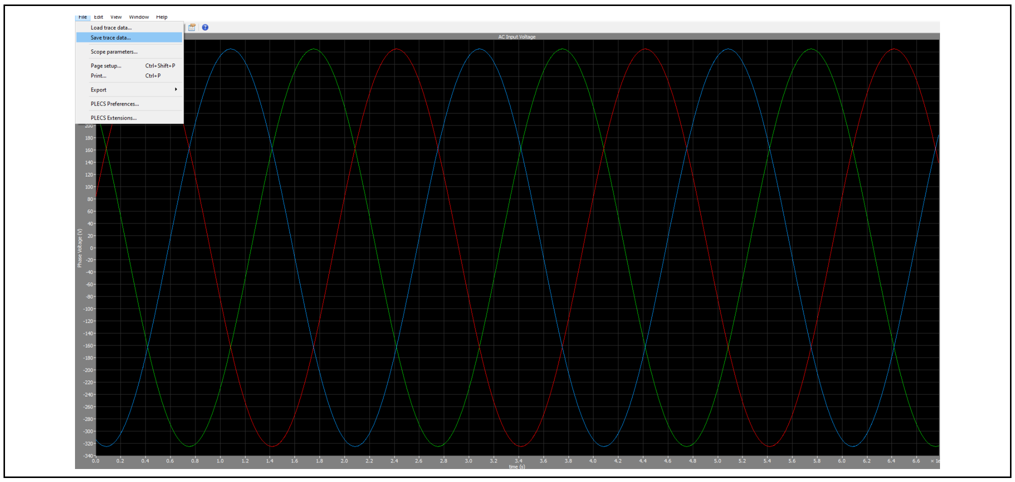

FIGURE 8-1: *Saving Scope Traces.*

The plot data can be exported into a pdf, bitmap, or csv file for reports or further analysis.

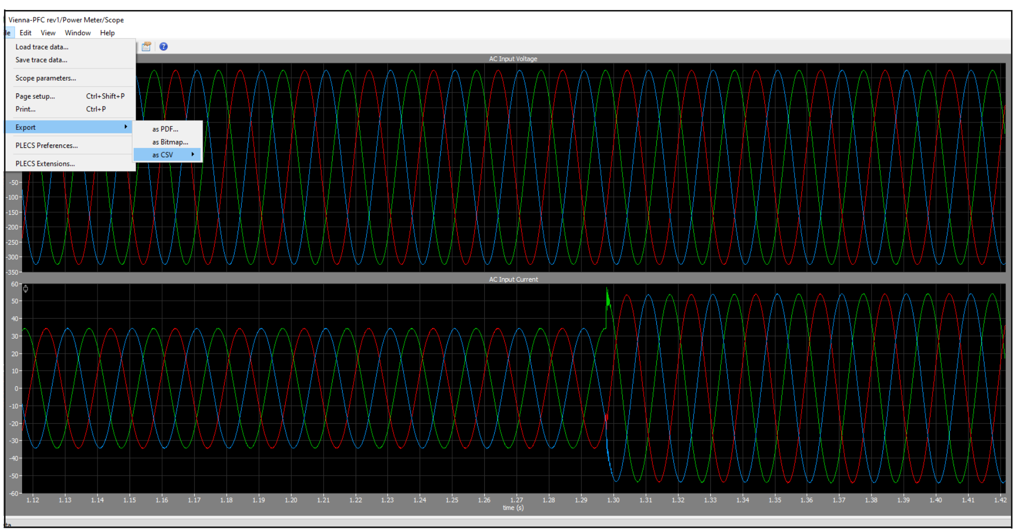

FIGURE 8-2: *Exporting Scope Traces.*

PLECS can display multiple traces from different simulation runs within the same session by using the Hold current trace button in the toolbar or by pressing the green plus button in the Traces window.

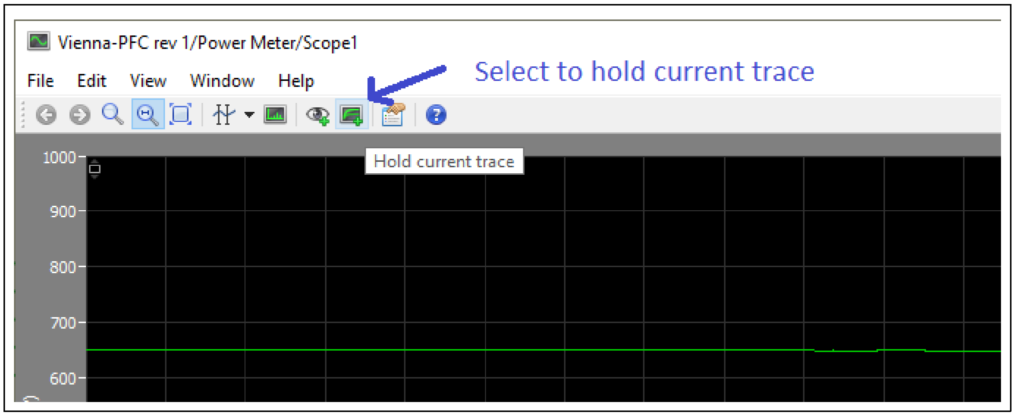

FIGURE 8-3: *Hold Current Trace.*

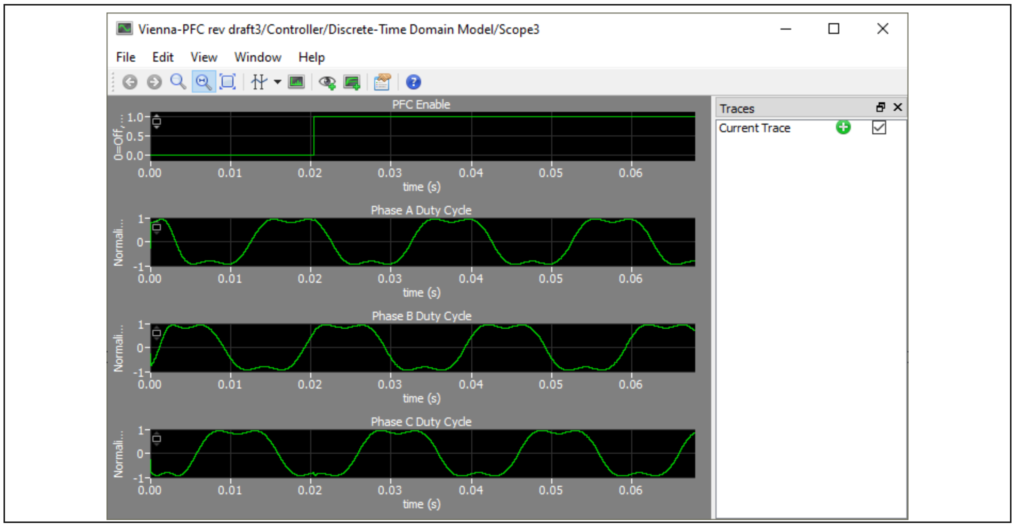

FIGURE 8-4: *Traces Window.*

PLECS MODEL QUICK START GUIDE FOR VIENNA PFC

Chapter 9. Power Meter

Included with the model is a power meter for displaying AC & DC voltage, current, and power as well as efficiency. It also includes a readout of the total switch losses and boost inductors core losses.

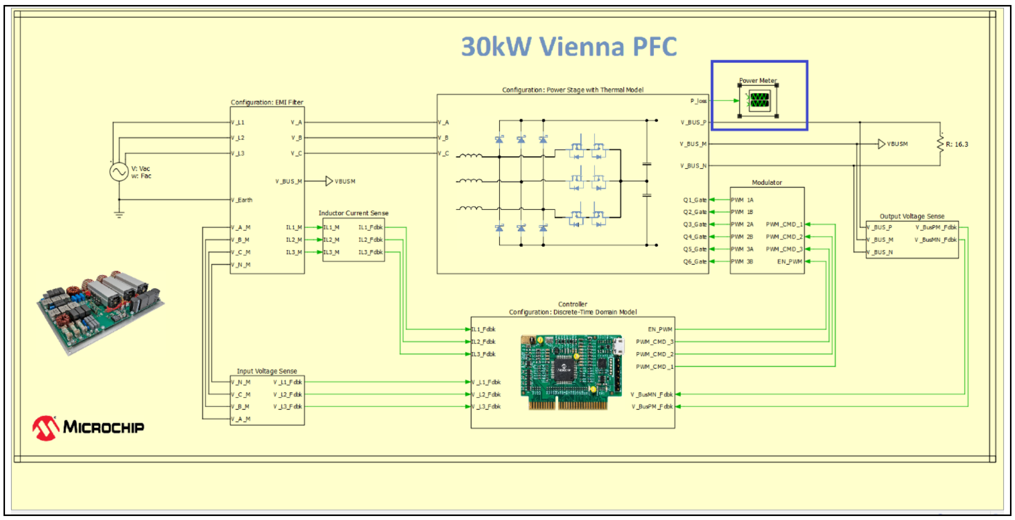

FIGURE 9-1: *Power Meter.*

In PLECS, switch and core losses are not simulated in the electrical domain. The SBD (Schottky barrier diode) and MOSFET conduction and switching losses are based on the thermal descriptions of the devices. The core losses are based on the core data sheet core-loss graph. Since the losses are not included in the electrical domain, they are added to the input power from the electrical domain for estimating total input power and efficiency. As such, the input current measurement does not include current from these losses.

The power meter includes filter blocks for averaging the data feeding the displays and scopes. The averaging window for the DC output voltage and current is set to 1ms. The remaining filters are set to 100ms. The filters introduce a delay in the readings. Therefore, the reading is value only after a steady state condition. The scopes also include instantaneous measurements.

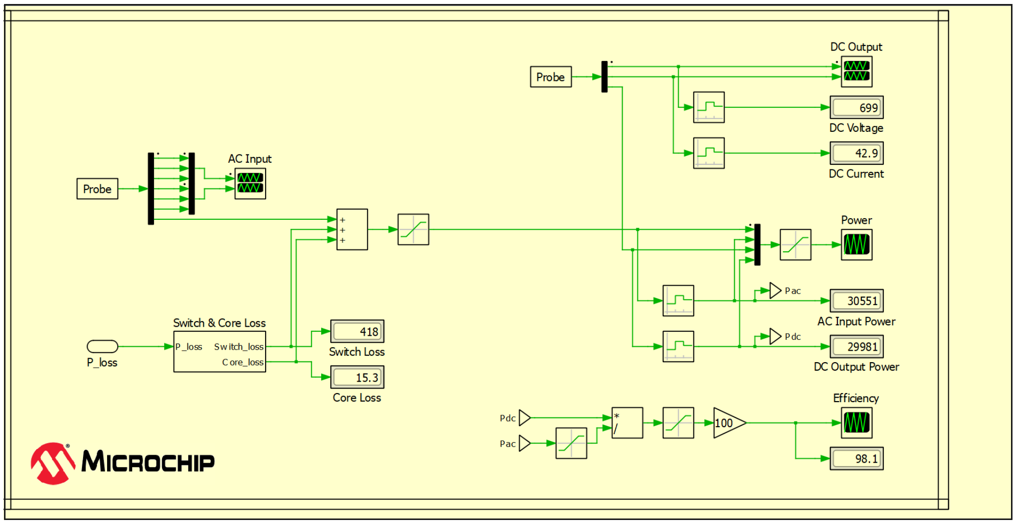

FIGURE 9-2: *Power Meter Subsystem.*

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