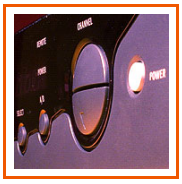
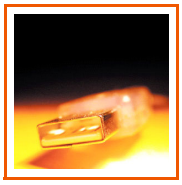
LAN9118

High-Performance Single-Chip 10/100 Non-PCI Ethernet Controller

PRODUCT FEATURES

Data Brief

Highlights

- Optimized for high-data rate applications such as video, high-definition video and multi-media applications
- Efficient architecture with low CPU overhead; easily interfaces to any CPU
- Reduces system and design costs

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital video recorders
- High definition televisions
- Digital music jukeboxes
- Digital media clients/servers
- DVD recorders/players
- Home gateways
- Video-over IP Solutions
- Wireless routers & access points
- IP PBX & video phones

Key Benefits

- Supports high and ultra-high performance applications
  - — Highest performing non-PCI Ethernet controller on the market
  - — 32-bit interface with very fast bus cycle times
  - — Burst-mode read mode
- Eliminates dropped packets
  - — Internal SRAM can store over 200 packets
  - — Supports automatic or host-triggered PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - — Supports Slave-DMA
  - — Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
  - — SRAM interface easily interfaces to any CPU or SoC
  - — Low-cost, low-pin count non-PCI interface for embedded designs
- Architected for Low Power
  - — Wake-on-LAN and Magic Packet Support with separate output pin
  - — Power-Management and multiple power-down modes

Specifications

- Integrated 10/100 MAC + PHY
- 802.3 compliant
- 16 kByte internal SRAM
- 2 Perfect Unicast + 16 Multicast Hash Filtering
- General Purpose Timer
- Supports external EEPROM
- 3LED/GPIO pins
- 3.3V Power Supply with 5V tolerant I/O
- 0 to 70°C
- Small form factor 100 pin TQFP package

ORDERING INFORMATION:

LAN9118-MD FOR 100 PIN, TQFP PACKAGE

LAN9118-MT FOR 100 PIN, LEAD-FREE TQFP PACKAGE

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

General Description

The LAN9118 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and low cost are required. The LAN9118 has been specifically architected to provide the highest performance possible for any given architecture. The LAN9118 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant.

The LAN9118 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16 and 32-bit microprocessors and microcontrollers. LAN9118 includes large transmit and receive data FIFO's with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9118 memory buffer architecture allows the most efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9118 is well suited for many high-performance embedded applications, including:

- Digital television
- Video record/playback systems
- Set-top boxes
- Printers and scanners

The LAN9118 supports numerous power management and wakeup features. The LAN9118 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including Magic Packet, Wake on LAN and Link Status Change. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

The LAN9118 also supports features which reduce or eliminate packet loss. Its internal 16k SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9118 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating a network collision. The host controller can also.

The diagram shown in Figure 1, "System Block Diagram utilizing the SMSC LAN9118", describes a typical system configuration of the LAN9118 in a typical embedded environment.

The LAN9118 is designed to be general purpose Ethernet controller that is platform independent. The LAN9118 consists of four major functional blocks. The four blocks are:

1. 10/100 Ethernet PHY
2. 10/100 Ethernet MAC
3. RX/TX FIFO's
4. Slave Interface Module

Block Diagrams

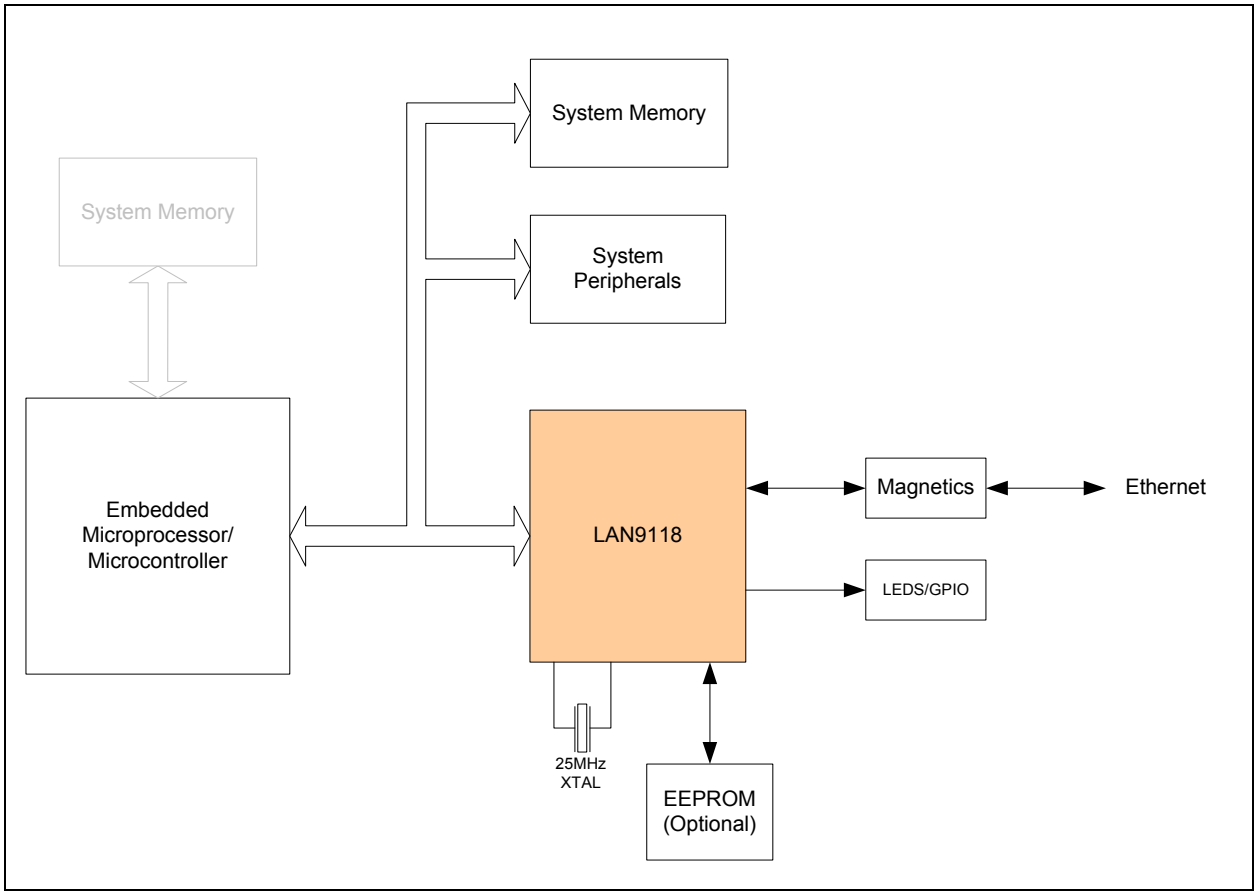


Figure 1 System Block Diagram utilizing the SMSC LAN9118

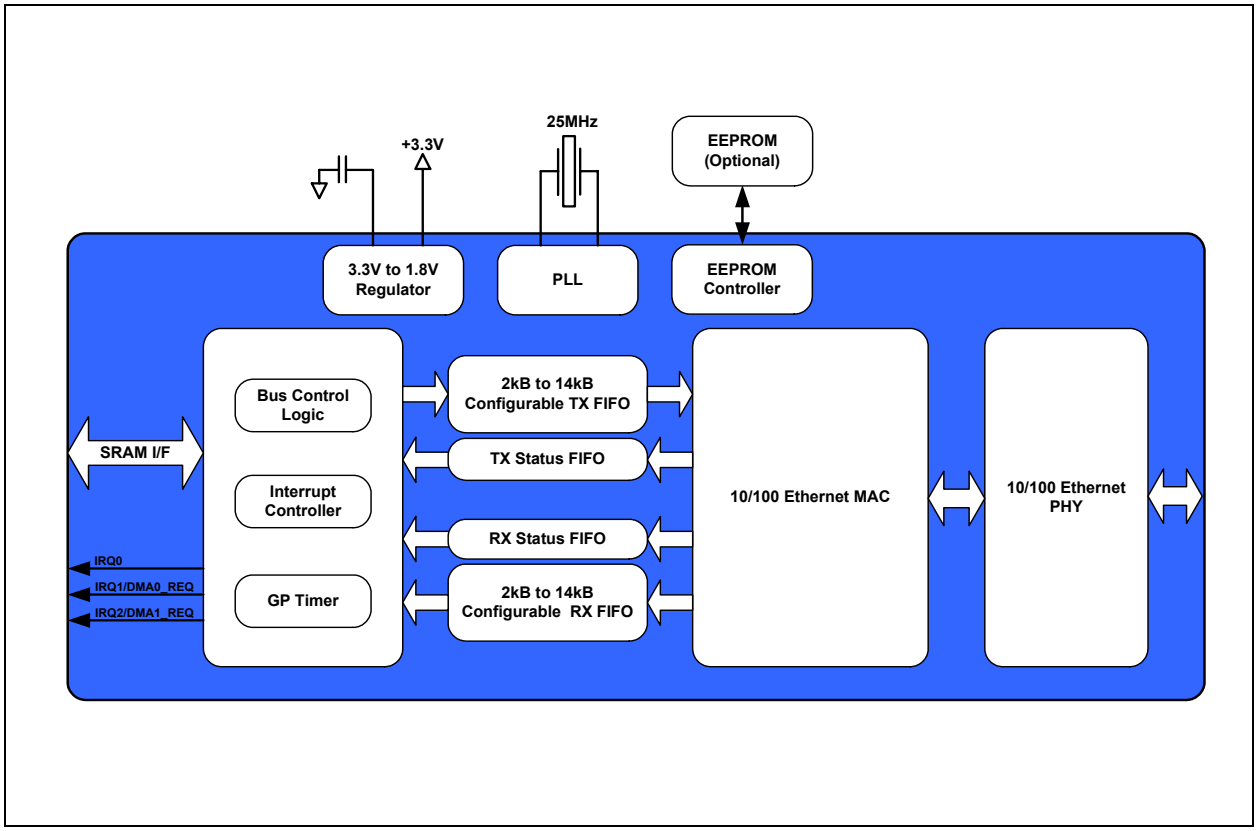


Figure 2 LAN9118 Internal Block Diagram

Package Outline

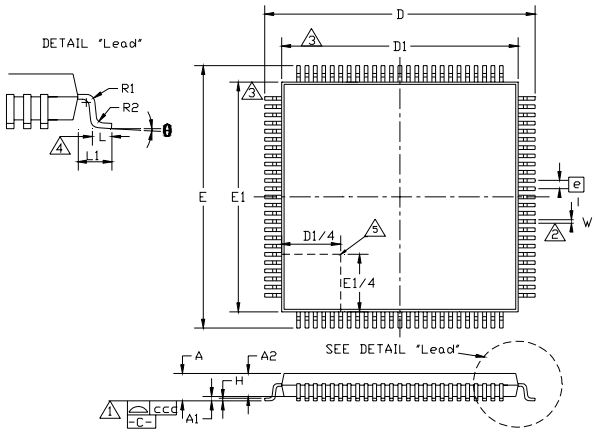


Figure 3 100 Pin TQFP Package Outline

Table 1 100 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

[1] Controlling Unit: millimeter.

[2] Tolerance on the true position of the leads is ± 0.04 mm maximum.

[3] Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.

[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

[5] Details of pin 1 identifier are optional but must be located within the zone indicated.