|  |
| --- |
| Microchip Technology Inc. |
| Second Generation SiC Spice Models |
| User’s Guide |

|  |
| --- |
| Dennis Meyer, Rev A  10-28-2020 |

# INTRODUCTION

Microchip SiC diode and MOSFET models are being replaced with a new generation of models. This should not be confused the generation of SiC. The first and second generation of Spice files are both for the “NextGen” devices.

First generation models emphasized model accuracy using relatively high-level math functions. The new generation has been developed specifically for model speed while bringing in better modeling accuracy and a wider device selection. The underlying math has changed substantially and should result in more stable simulations.

## Model Interface Overview

The obsolete first-generation Spice files consisted of three diode libraries and three MOSFET libraries.

|  |  |
| --- | --- |
| MSC0xxSDA070.lib | Diode 700V basic and thermal model |
| MSC0xxSDA120.lib | Diode 1200V basic and thermal model |
| MSC0xxSDA170.lib | Diode 1700V basic and thermal model |
| MSCxxxSMA070.lib | MOSFET 700V basic and thermal model |
| MSCxxxSMA120.lib | MOSFET 1200V basic and thermal model |
| MSCxxxSMA170.lib | MOSFET 1700V basic and thermal model |

First generation sub-circuit models are called in the following manner.

|  |  |
| --- | --- |
| Model | Spice Argument |
| Diode basic | Xxx A\_node C\_node *partnumber* |
| Diode thermal | Xxx A\_node C\_node Tj\_node, Tc\_node *parnumber*T |
| MOSFET basic | Xxx D\_node G\_node S\_node *partnumber* |
| MOSFET thermal | Xxx D\_node G\_node S\_node Tj\_node, Tc\_node *parnumber*T |
| MOSFET Kelvin basic | Xxx D\_node G\_node GK\_node S\_node *partnumber* |
| MOSFET Kelvin thermal | Xxx D\_node G\_node GK\_node S\_node Tj\_node, Tc\_node *parnumber*T |

The second-generation file naming is as follows:

|  |  |
| --- | --- |
| MSCSDA070\_L1.lib | Diode 700V basic model |
| MSCSDA070\_L2.lib | Diode 700V thermal model |
| MSCSDA120\_L1.lib | Diode 1200V basic model |
| MSCSDA120\_L2.lib | Diode 1200V thermal model |
| MSCSDA170\_L1.lib | Diode 1700V basic model |
| MSCSDA170\_L2.lib | Diode 1700V thermal model |
| MSCSMA070\_L1.lib | MOSFET 700V basic model |
| MSCSMA070\_L2.lib | MOSFET 700V thermal model |
| MSCSMA120\_L1.lib | MOSFET 1200V basic model |
| MSCSMA120\_L2.lib | MOSFET 1200V thermal model |
| MSCSMA170\_L1.lib | MOSFET 1700V basic model |
| MSCSMA170\_L2.lib | MOSFET 1700V thermal model |

Second generation sub-circuit models are called in the following manner.

|  |  |
| --- | --- |
| Model | Spice Argument |
| Diode basic | Xxx A\_node C\_node *partnumber*\_L1 PARAMS: <*see below*> |
| Diode thermal | Xxx A\_node C\_node Tj\_node, Tc\_node *parnumber*\_L2 PARAMS: <*see below*> |
| MOSFET basic | Xxx D\_node G\_node S\_node *partnumber*\_L1 PARAMS: <*see below*> |
| MOSFET thermal | Xxx D\_node G\_node S\_node Tj\_node, Tc\_node *parnumber*\_L2 PARAMS: <*see below*> |
| MOSFET Kelvin basic | Xxx D\_node G\_node GK\_node S\_node *partnumber*\_L1 PARAMS: <*see below*> |
| MOSFET Kelvin thermal | Xxx D\_node G\_node GK\_node S\_node Tj\_node, Tc\_node *parnumber*\_L2 PARAMS: <*see below*> |

Arguments that can be brought in through the PARAMS statement are as follows:

TEMP=xx Set the junction temperature, degrees C. L1 model only.

GM=1 This sets the transconductance relative to the die sized scaled value. It is a relative value that may range from about 0.9 to 1.1. This variable would normally be used to introduce threshold differences when doing module simulation:

VTO=2 Most of the models have been setup with a 25C threshold of about 2V. This does not relate to the data sheet threshold rather it is specific to the Spice curve fitting. This variable would normally be used to introduce threshold differences when doing module simulation:

## Second Generation Level 1, Level 2 Library Differences

Device models use equations to simulate diode and channel conductions. Most parameters in these equations are temperature dependent.

L1 Spice models precompile the temperature into the model and then treat the temperature as a constant. The temperature can be modified in the parameter argument. This is the conventional way temperature variability is treated in Spice. It is done this way to relieve the differential equation solver of the burden of calculating temperature dependent parameters.

L2 Spice models treat the temperature and all resulting device parameters as variables. The temperature changes slowly in a simulation which means a meaningful thermal simulation has a long run time. Package models have a package resistive and capacitive Foster model between the Tj pin and the Tc pin.

The Tj pin sources a current of 1A/W. Foster model capacitors have a value of 1 F to 1 Joule/C. Some simulators can calculate overall package dissipation. This function will not work when the Foster model is included in the device.

With die models the thermal conductivity is not modeled. Die model have a 1 ohm resistor between the Tj and Tc pin as a place holder to make the higher level schematic pinout compatible with the packaged devices. All modeling would be external using the Tj pin.

The L2 Foster model requires that the Tc pin be tied to a voltage (temperature). The Foster model is not valid with connected to an outside network. That is because the translation from Foster to Cauer requires that the external network be included to do the translation. Microchip should be contacted for assistance if higher level simulation is required.

## Reverse Recovery

Body diode reverse recovery presents a difficult problem in Spice like simulators. This is because it is a very complex process. Most models across the industry model it very poorly with both Si and SiC devices although it may be possible to do reasonably with SiC. If this is added in the future it will be as another level device model.

With 700V MOSFETs the drift region is very shallow. The body diode has a slight effect on switching loss that can be covered by padding the calculated losses with about a 20-30% switching loss margin at higher temperatures. With higher voltage devices it is recommended that switching loss be based on the graphs in the device data sheet by interpolating to the operating point.

# GETTING STARTED

Adding a transistor or diode model to a schematic or netlist requires two things:

* Include the necessary library to the design.
* Reference either by symbol or text to the transistor or diode to be modeled.

Spice is a case insensitive text-based language. Various schematic editors, such as LTSpice, PSpice, etc., are built upon this to present a more user-friendly interface. The symbolic schematic is not part of the Spice complier, it is a layer over it. The first stage in simulation is translating the symbolic schematic to a netlist. Then the netlist is then acted upon by the Spice simulator.

## Adding a Library to a Schematic

Symbolic schematics will always have a way to insert Spice native commands. To add a library add the following to the schematic:

include ‘*filename*’

Path references are generally allowed. As an example, a reference to the 700V L1 library in a directory adjacent to the library directory would be referenced as:

include ‘../*library\_directory*/MSCSMA070\_L1.lib’

The quote marks are required in the listing.

## Adding a Device to a Schematic

The models are inserted into a schematic as sub-circuits. From section 1.2, the following line is shown to insert a three-lead level 1 MOSFET:

Xxx D\_node G\_node S\_node *partnumber*\_L1 PARAMS: …

Xxx is the reference. It must start with an ‘X’ indicating it is a reference to a sub-circuit. The lower case ‘xx’ can be a text or number string, normally the reference designator.

The following three entries are the drain, gate, and source net names. Following that is the sub-circuit name. It must match to a sub-circuit in the library.

Following that are optional parameters used to modify the subcircuit. They can be used to individually modify a sub-circuit to make it different than other models of the same transistor. As an example, the following will add a MSC025SMA120B level 1 model to a schematic with a 10% higher transconductance than normal. It has a drain connection to node 20, gate to node 30, and source to node 40. It simulates at 35C. Nodes can be any combination of letters and numbers:

X10 DrainNet GateNet SourceNet MSC025SMA120B\_L1 PARAMS:GM=1.1 TEMP=35

If a text entry like this is used then the nodes attaching to the model should be labeled on the schematic, as against letting the software pick a label, as is done with unlabeled nets.

The above transistor can also be referenced through a symbol. As an example, in LTSpice the 3 lead MOSFET model, “nmos”, can be added to a schematic. After doing this use CNTRL, RClick to view the Component Attribute Editor. Make the following edits:

* Change the prefix to X
* In the value field place the part number, MSC025SMA120B\_L1 in the case above.
* In the “Value2” field add PARAMS: GM=1.1 TEMP=35

The net name ordering on the symbol must match the net ordering in the model. Other than that, the symbol name does not matter.

## Simulator Settings

Spice can be difficult at times. Problems with convergence are the most common problem. There is a very good article at Intusoft, <http://www.intusoft.com/articles/converg.pdf>, that describes how to deal with problems with convergence and give many great recommendations.

As a starting point it is recommended that the following options be applied in Spice.

.options *ABSTOL=1n*

*.options CHGTOL=1p*

*.options ITL1=150*

*.options ITL2=150*

*.options ITL4=500*

*.options RELTOL=0.001*

With LTSpice the alternate solver sometimes works better. It is accessed through the Tool tab, SPICE/Solver.