



3-Phase 30 kW Vienna PFC Reference Design

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXXXA”, where “XXXXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, visit www.microchip.com/PFC and www.microchip.com/SiC for general SiC information.

INTRODUCTION

This chapter contains general information that will be useful to know before using the 3-Phase 30 kW Vienna PFC Reference Design. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [Recommended Reading](#)
- [The Microchip Website](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document describes how to use the 3-Phase 30 kW Vienna PFC Reference Design (part number MSCSICPFC/REF5) as a development tool. The manual layout is as follows:

- **Chapter 1. “Reference Design Overview”** – Important information about the 3-Phase 30 kW Vienna PFC Reference Design.
- **Chapter 2. “Circuit Operation”** – Includes description of and instructions regarding the circuitry of the 3-Phase 30 kW Vienna PFC Reference Design.
- **Chapter 3. “Testing and Results”** – Important information about the efficiency of the 3-Phase 30 kW Vienna PFC Reference Design.
- **Chapter 4. “Thermal Design”** – Important information about the heatsinking required for the SiC MOSFETs.
- **Chapter 5. “Mechanical Design and Assembly”** – Important information about the methods of attachment and the mechanical aspects of the evaluation board assembly.

3-Phase 30 kW Vienna PFC Reference Design

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

RECOMMENDED READING

This user's guide describes how to use the 3-Phase 30 kW Vienna PFC Reference Design (part number MSCSICPFC/REF5). Firmware and additional documentation can be found on the Microchip Vienna PFC reference design product page at this link: www.microchip.com/PFC.

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- Technical Support

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To learn more about the Vienna PFC Reference Design and SiC products from Microchip, visit www.microchip.com/SiC.

DOCUMENT REVISION HISTORY

Revision B (July 2020)

- Updated [Section 1.2 “Reference Design Overview”](#).
- Updated [Section 1.3 “Feature Summary”](#).
- Updated [Table 2-1](#).
- Updated [Figure 2-10](#).
- Updated [Section 2.7.2 “Level Shifting, Attenuation and Filtering”](#).
- Updated [Figure 2-11](#).
- Updated [Section 4.1 “Introduction”](#).
- Updated [Figure 4-1](#).
- Added [Figure 4-2](#).

Revision A (February 2020)

- Initial release of this document.

Chapter 1. Reference Design Overview

1.1 INTRODUCTION

This chapter provides an overview of the 3-Phase 30 kW Vienna PFC Reference Design and covers the following topics:

- [Reference Design Overview](#)
- [Feature Summary](#)
- [Electrical Specifications](#)
- [Power-up and Power-Down Procedures](#)

Please note only the design files are being offered. Hardware is not available through Microchip.

1.2 REFERENCE DESIGN OVERVIEW

This platform is a three-phase Vienna PFC reference design for use in Hybrid Electric Vehicle (HEV) and Electric Vehicle (EV) chargers, and high-power Switch Mode Power Supply (SMPS) applications. This reference design achieves 98.6% efficiency at 30 kW output power using Microchip's 700V, 15 m Ω SiC MOSFETs (MSC015SMA070B) and 1200V, 50A SiC Schottky Barrier Diodes (MSC050SDA120B).

1.2.1 3-Phase 30 kW Vienna PFC Reference Design Advantages Over Standard 3-Phase Boost

- Reduced voltage stress on the switching SiC MOSFETs
- Lower switching loss
- Higher operating frequency – smaller magnetics
- Lower Common-mode emissions

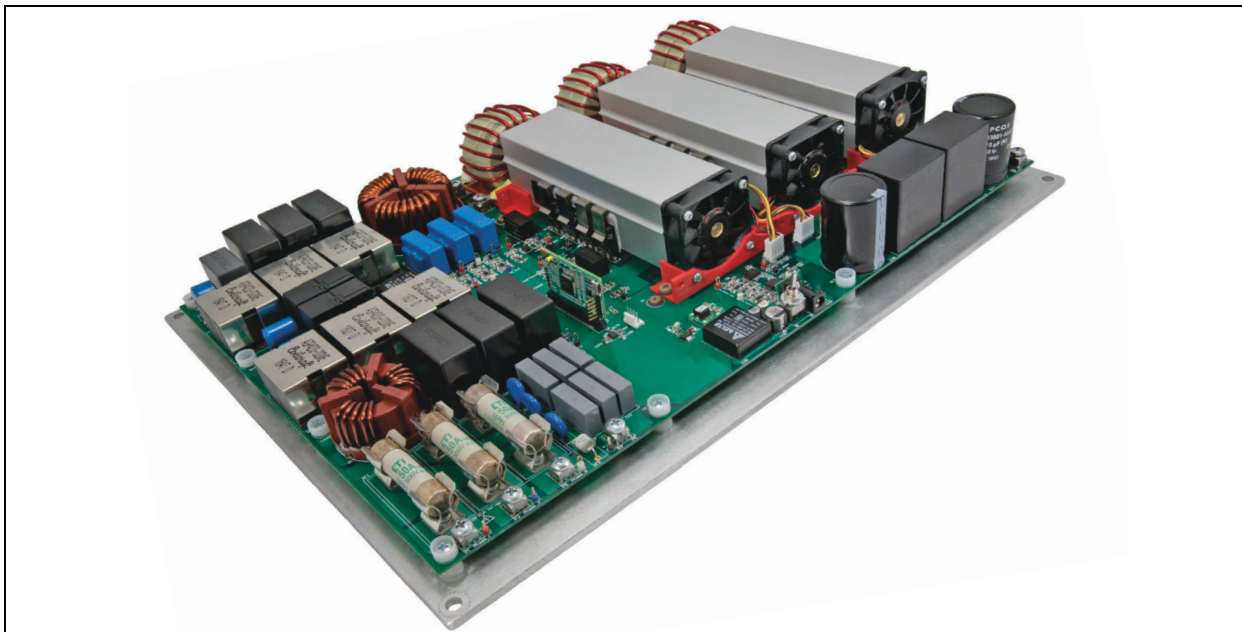


FIGURE 1-1: 30 kW Vienna PFC Evaluation Board.

1.3 FEATURE SUMMARY

- 30 kW Vienna rectifier topology with Microchip 700V, 15 mΩ SiC MOSFETs and 1200V, 50A SiC Schottky Barrier Diodes (SBDs)
- Three-phase, 380/400 V_{RMS}, 50 Hz or 60 Hz input voltage
- 700 V_{DC} output voltage
- 140 kHz switching frequency reduces magnetics size
- Full-power output at +40°C ambient temperature
- Digitally controlled current and voltage loop using a Microchip dual core dsPIC33CH microcontroller
- Digital control reduces harmonics and eases upgrades
- Dedicated Common-mode and Differential-mode filters are adopted
- Verified open source software for the digital control using cost-effective, three-level modulation without need of FPGA
- Well-designed cooling channel with integrated fan to reduce the thermal resistance and total size
- SiC devices mounted on the closest sides of heat sink to reduce commutation loop inductance and the associated voltage spikes across the power devices
- Aluminum Nitride (AlN) spacers meant for SiC semiconductors to reduce parasitic capacitance and Common-mode noise
- Well designed PCB layout with considerations for safety, current stress, mechanical stress and noise immunity

1.4 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Parameter	Specification
Input Voltage (V _{RMS(L-L)})	Three-Phase Input 380V, 50 Hz (Typical Asia)
	Three-Phase Input 400V, 50 Hz (Typical Europe)
Input Current (A _{RMS})	46 A _{RMS} @ 380 V _{RMS} Input, P _{OUT} = 30 kW
	44 A _{RMS} @ 400 V _{RMS} Input, P _{OUT} = 30 kW
Output Voltage	700 V _{DC} Nominal
Output Power	30 kW @ 380V/400V Input
Efficiency	98.5% @ 380V/400V Input, 30 kW Output Power
PWM Switching Frequency	140 kHz
THD	2.5% @ 380V/400 V _{RMS} , 30 kW Output Power
	4.3% @ 400 V _{RMS} , 16 kW P _{OUT}
Bias Voltage Input	12V/2A

3-Phase 30 kW Vienna PFC Reference Design

1.5 POWER-UP AND POWER-DOWN PROCEDURES

WARNING

The Power-up Procedure described below must be followed to prevent damage to the circuitry.

CAUTION

The voltages that are accessible in this design are hazardous and present a significant risk of serious injury.

In addition to the shock hazard, the voltages, currents and power levels of this board may present fire or other hazards if not properly operated.

Only properly trained and qualified personnel should be allowed to test and operate this design.

Please use the necessary and appropriate techniques to avoid injury and/or property damage.

Make sure the input power service has enough ampacity (maximum current carrying capacity) to supply steady-state and inrush current to the evaluation board when the output is fully loaded.

1.5.1 Power-up Procedure

Note: Additional start-up information can be found in [Section 2.11 “Start-up Process”](#).

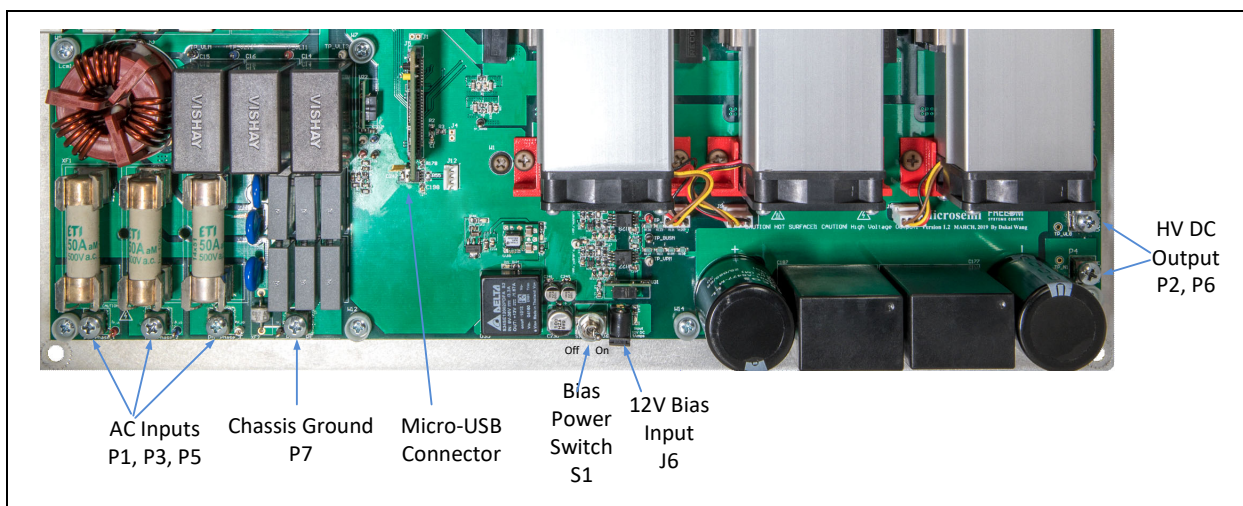


FIGURE 1-2: Input and Output Connections.

1. Make sure connector P7 is connected to an earth ground.
2. Connect a load to high-voltage output connectors, P2 (positive) and P6 (return). Make sure the load is off.
3. Apply a 12V bias to connector J6. The bias supply should have a current rating of 2A. The green LED should be lit up. Turn on the switch, S1. Make sure the fans on each of the three heat sinks are operating properly.
4. Connect a Micro-USB cable between a computer and connector J3 on the dsPIC® DSC PIM board. A terminal program is used to turn the inrush current relay on and off. UART settings are: Baud Rate = 115200; Data Bits = 8; Parity = None.

5. Using the terminal program, send Hex 33 (0x33) to ensure the relays across the inrush resistors are open.
6. Apply 380V or 400V (depending on input requirements) 3-phase AC voltage to the input terminals (P1, P3, P5).
7. Inrush resistors will limit the current that charges up the output capacitors when the AC voltage is applied.
8. Once the 3-phase AC voltage is applied, the inrush relays can be closed by sending Hex 3B (0x3B). This bypasses the inrush resistors.
9. Apply a small load, greater than 500W, to the output. This will prevent the output capacitors from an overvoltage condition when the Vienna PFC supply starts switching.
10. Using the terminal program, send Hex 55 (0x55), which turns on the controller and starts the process of boosting the output voltage to $700 V_{DC}$. Once the power supply is running, different load conditions can be applied to the output. A minimum load must always be applied to the output to prevent overcharging and damage to the power supply.

1.5.2 Power-Down Procedure

1. Lower the output load to around 500W.
2. Remove the AC input voltage or turn off the controller by sending Hex AA (0xAA) from the terminal program.
3. If the terminal program was used to turn off the power supply, the AC input voltage should be turned off.
4. Remove the output load.

Note: Keeping a small load on the output until the AC is removed helps to quickly discharge the output capacitors.

5. Using the terminal program, send Hex 33 (0x33) to open the inrush relays.
6. Turn off switch S1 and remove the 12V bias supply voltage.

WARNING

After the power supply is turned off, it is important to make sure all high-voltage (input and output) capacitors have been safely discharged.

It is important to measure the voltage on these parts before touching or working on the board.

Failure to do so can result in personal injury and/or damage to the board or test equipment.

2.1 CIRCUIT DESCRIPTION

The SiC MOSFET switching is controlled by a digital controller and 3-level modulation scheme to force sinusoidal input currents that are in-phase with the input voltages.

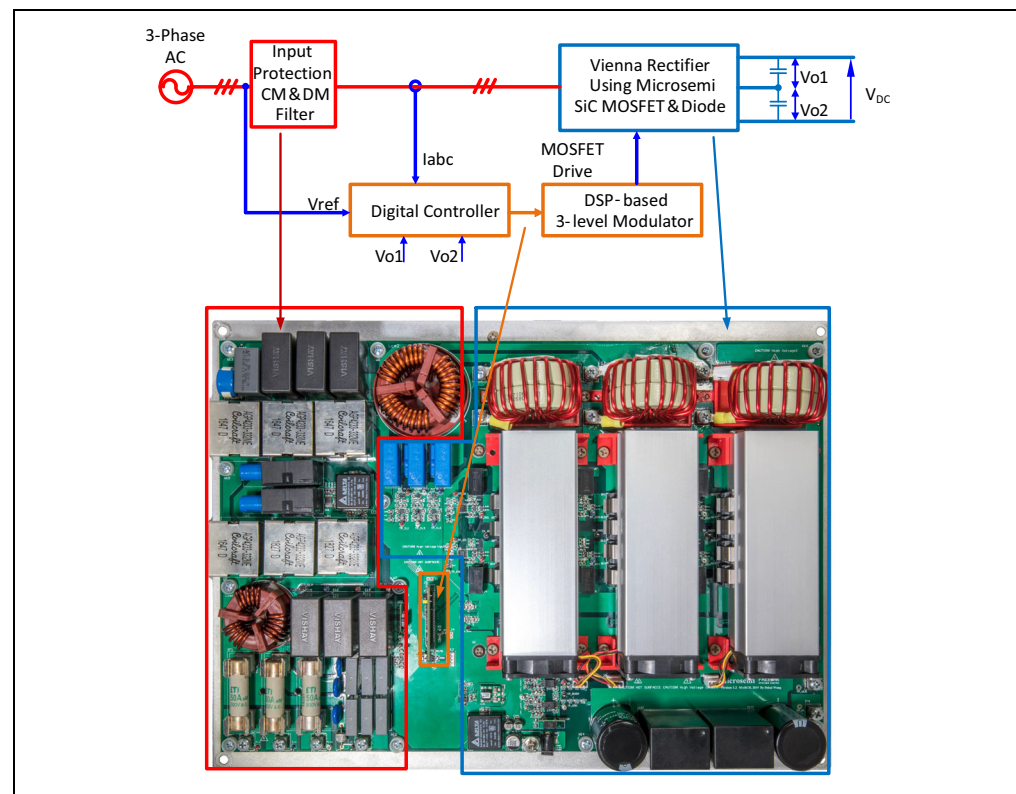


FIGURE 2-1: *Block Diagram.*

2.2 THREE-LEVEL MODE OF OPERATION

This topology has a 3-level characteristic, as defined by the three possible states of the neutral point switch (see Figure 2-2). These three states are determined by the switch status (on or off) and the input current flow direction.

Using Phase A as an example, the voltage across the pair of series connected SiC MOSFETs ($v_a - V_{BUS_M}$) can be:

1. $\sim 0V$ when QA1 and/or QA2 are on.
2. $+V_{DC}/2$ when QA1 and QA2 are off, and input current is flowing in the positive direction, into the phase node. For this condition, SiC diode DA1 is conducting and the phase node is clamped to V_{DC} .
3. $-V_{DC}/2$ when QA1 and QA2 are off, and input current is flowing in the negative direction, out of the phase node. For this condition, SiC diode DA2 is conducting and the phase node is clamped to the DC bus return.

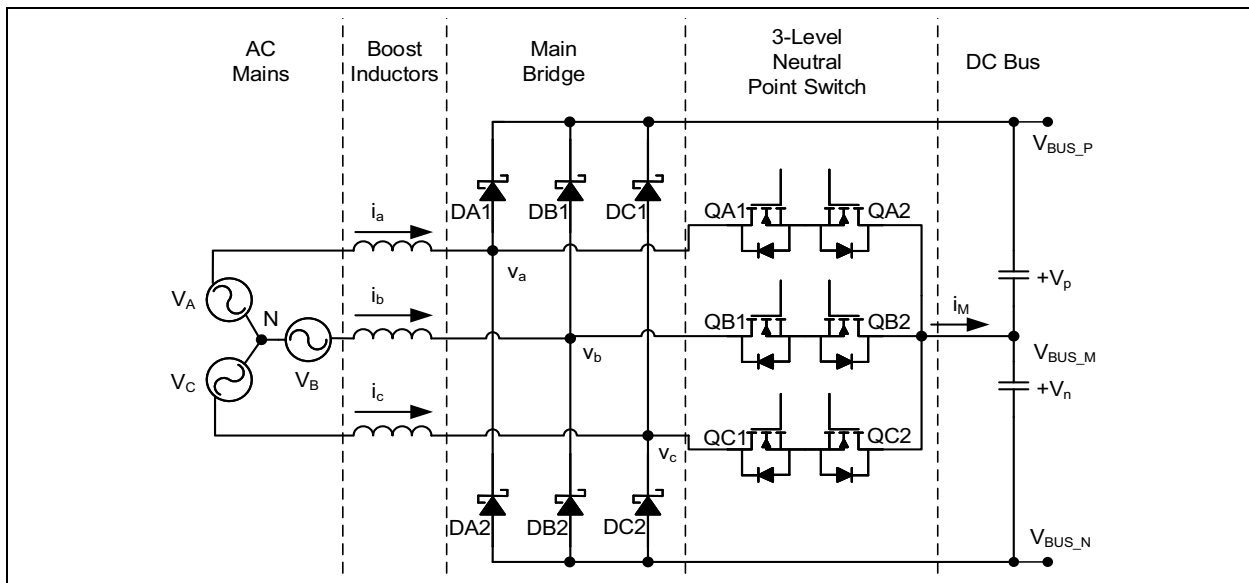


FIGURE 2-2: Simplified Power Stage Schematic.

2.3 POWER STAGE OPERATION

The simplified power stage diagram, shown in Figure 2-2, will be used to illustrate the basic operation of the Vienna rectifier. V_A , V_B and V_C are the AC voltages of a Y connected 3-phase input. Each of these voltages are equal in magnitude and frequency, but shifted in-phase by 120° . This example will focus on Phase A, but the power stage and switching operation is identical to Phases B and C.

The node v_a can be in any of three states, depending on the polarity of the input, V_A , and the ON/OFF state of the switch (QA1 and QA2) when in steady-state operation:

1. Regardless of the input polarity, when the switch is on, $v_a = V_{BUS_M}$; the midpoint voltage of the output voltage capacitors.
2. When the switch is off and V_A is positive, inductor current, i_a , flows into node v_a and SiC diode DA1 conducts. For this case, $v_a = V_{BUS_P}$.
3. When the switch is off and V_A is negative, inductor current, i_a , flows out of node v_a (into source V_A) and SiC diode DA2 conducts. For this case, $v_a = V_{BUS_N}$.

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2.4 POWER STAGE CALCULATIONS

Term Definitions:

$V_A(t)$, $V_B(t)$ and $V_C(t)$ are the instantaneous line to neutral sinusoidal input voltages with a frequency of $\frac{\omega_0}{2\pi}$.

V_M is the peak input (line/neutral) voltage. Each of these three phases is assumed to have the same peak (or RMS) amplitude and are equally offset in-phase by 120° .

$$V_A(t) = V_M \times \sin(\omega_0 \times t)$$

$$V_B(t) = V_M \times \sin\left(\omega_0 \times t - \frac{2 \times \pi}{3}\right)$$

$$V_C(t) = V_M \times \sin\left(\omega_0 \times t + \frac{2 \times \pi}{3}\right)$$

Input power depends on the output power and the efficiency (η) of the converter.

$$P_{OUT} = P_{IN} \times \eta$$

$I_{IN(PK)}$ is the peak input line current (A).

EQUATION 2-1: PEAK INPUT LINE CURRENT

$$I_{IN(PK)} = \frac{\sqrt{2} \times P_{IN}}{\sqrt{3} \times PF \times V_{IN_LL(RMS)}}$$

EQUATION 2-2: MODULATION INDEX – M

$$M = \frac{V_{DC}}{\sqrt{3} \cdot V_{IN_LN(PK)}}$$

Where:

PF = Input Power Factor

P_{IN} = Total 3-Phase Input Power

$V_{IN_LL(RMS)}$ = RMS Line to Line Voltage

$V_{IN_LN(PK)}$ = Peak Line to Neutral Voltage

V_{DC} = DC Voltage at the Output

2.4.1 SiC Diode Calculations

For the six SBD rectifiers, the average and RMS forward currents are calculated with [Equation 2-3](#) and [Equation 2-4](#).

EQUATION 2-3: AVERAGE CURRENT

$$I_{D(AVE)} = \frac{I_{IN(PK)}}{2 \times \sqrt{3} \times M}$$

EQUATION 2-4: RMS CURRENT

$$I_{D(RMS)} = I_{IN(PK)} \times \sqrt{\frac{4}{3 \times \sqrt{3} \times \pi \times M}}$$

The average power dissipated in the SiC diode is calculated using the average diode current ($I_{D(AVE)}$) x the forward voltage drop at $I_{D(AVE)}$.

$$P_{D(AVE)} = I_{D(AVE)} \times V_F$$

The power dissipation in the SiC Schottky diode due to junction capacitance is relatively small and is ignored in this calculation.

2.4.2 SiC MOSFET Calculations

In this version of the Vienna PFC rectifier, there is one bidirectional switch per phase. The bidirectional switch consists of two SiC MOSFETs connected in series with a common source, as shown in Figure 2-3. The common source reduces the driver complexity and cost.

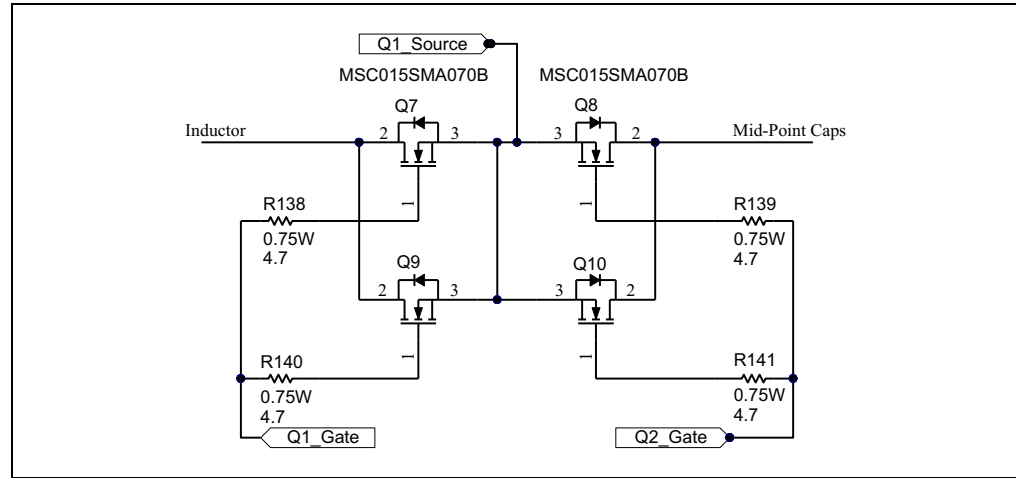


FIGURE 2-3: Bidirectional SiC MOSFET Switch.

At the 30 kW power level, each phase requires two bidirectional switches in parallel to reduce power dissipation in the switch and improve efficiency. The current and power calculations shown in Equation 2-5 and Equation 2-6 are for each leg of the rectifier. It is assumed that the calculated currents and power dissipation are divided evenly amongst the SiC MOSFETs in parallel.

EQUATION 2-5: MOSFET AVERAGE CURRENT

$$I_{MOSFET(AVE)} = I_{IN(PK)} \times \left(\frac{2}{\pi} - \frac{1}{\sqrt{3} \times M} \right)$$

EQUATION 2-6: MOSFET RMS CURRENT

$$I_{MOSFET(RMS)} = I_{IN(PK)} \times \sqrt{\frac{1}{2} - \frac{8}{3 \times \sqrt{3} \times \pi \times M}}$$

The power dissipated in the SiC MOSFET is the sum of the on-time (conduction) losses due to $R_{DS(ON)}$, and the switching losses due to turn-on and turn-off power dissipation:

$$P_{FET} = P_{FET(COND)} + P_{Switch(On)} + P_{Switch(Off)}$$

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2.4.2.1 CONDUCTION LOSS

Each SiC MOSFET dissipates power during both the positive and negative input cycle. Referring to [Figure 2-3](#), SiC MOSFETs' Q7/Q9 are switching during a positive AC input cycle. To improve efficiency, SiC MOSFETs' Q8/Q10 are turned on (not switching) during the entire positive AC input cycle. This bypasses the body diode conduction and reduces power dissipation in the SiC MOSFET. Conversely, during the negative AC input cycle, SiC MOSFETs' Q8/Q10 are switched and Q7/Q9 are turned on.

When calculating conduction loss, power dissipation in both the positive and negative AC input cycles must be accounted for.

EQUATION 2-7: CONDUCTION LOSS

$$P_{FET(COND)} = I_{MOSFET(RMS)}^2 \times R_{DS(ON)}$$

Where:

$P_{FET(COND)}$ = Conduction ($R_{D(SON)}$) Loss for Either Q7/Q9 Pair or Q8/Q10 Pair

2.4.2.2 SWITCHING LOSS

Switching loss in a SiC MOSFET occurs when V_{DS} and I_D are simultaneously present during turn-on and turn-off. The power dissipation due to switching depends on voltage, current, switching frequency and t_R , t_F . Switching loss in topologies with a constant switched current can easily be calculated. However, the peak SiC MOSFET current in the Vienna PFC is modulated by the sinusoidal nature of the AC input and by the 3rd harmonic frequency that is injected into the control signal for improved harmonic rejection. Due to this occurrence, the switching loss is more accurately simulated than calculated. Nonetheless, switching loss can be approximated by [Equation 2-8](#) and [Equation 2-9](#), which estimate switching loss using the SiC MOSFETs' rise and fall time. In these equations, one half of the SiC MOSFET average current is used because the SiC MOSFET is only switching for half of the AC input period. During the other half, the SiC MOSFET is turned on (without switching).

EQUATION 2-8: TURN-ON SWITCHING LOSS

$$P_{Switch(ON)} = 0.5 \times V_{DS(FET)} \times \frac{I_{MOSFET(AVE)}}{2} \times t_R \times f_{SW}$$

Where:

$V_{DS(FET)}$ = $0.5 \times V_{DC}$ (half the output voltage)

$I_{MOSFET(AVE)}$ = Average SiC MOSFET Current Calculated Above

t_R = SiC MOSFET Turn-On Time

f_{SW} = SiC MOSFET Switching Frequency

EQUATION 2-9: TURN-OFF SWITCHING LOSS

$$P_{Switch(OFF)} = 0.5 \times V_{DS(FET)} \times \frac{I_{MOSFET(AVE)}}{2} \times t_F \times f_{SW}$$

Where:

$V_{DS(FET)}$ = $0.5 \times V_{DC}$ (half the output voltage)

$I_{MOSFET(AVE)}$ = Average SiC MOSFET Current Calculated Above

t_F = SiC MOSFET Turn-Off Time

f_{SW} = SiC MOSFET Switching Frequency

2.4.3 Output Capacitor Calculations

The output capacitor RMS current is calculated with [Equation 2-10](#).

EQUATION 2-10: OUTPUT CAPACITOR RMS CURRENT

$$I_{COUT(RMS)} = I_{IN(PK)} \times \sqrt{\frac{5}{2 \times \pi \times M} - \frac{3}{4 \times M^2}}$$

The RMS current is the same in both the upper and lower output capacitors.

Power dissipation in the capacitors is calculated with [Equation 2-11](#).

EQUATION 2-11: OUTPUT CAPACITOR POWER DISSIPATION

$$P_{(COUT)} = I_{COUT(RMS)}^2 \times R_{ESR}$$

Where:

R_{ESR} = Output Capacitor's ESR

2.4.4 Boost Inductor

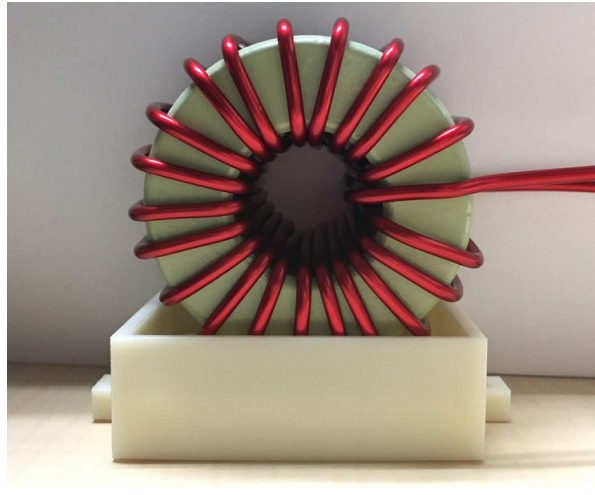


FIGURE 2-4: Boost Inductor.

3-Phase 30 kW Vienna PFC Reference Design

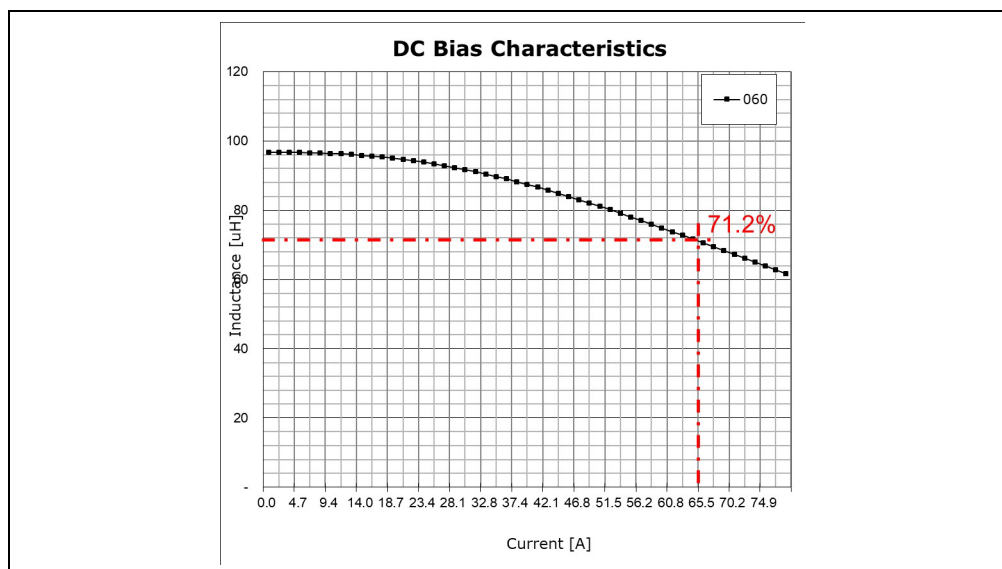


FIGURE 2-5: Characteristics.

Table 2-1 summarizes the boost inductor's parameters. At full power (30 kW), winding (copper) loss is 15.2W and core loss is 5.2W, for a total of 20.4W of power dissipated in each inductor.

TABLE 2-1: BOOST INDUCTOR CORE AND WINDING SPECIFICATIONS

Parameter	Value
Core Vendor and P/N	Chang Sung: CH-571060 Magnetics: 58192_A2
Material	CH (High Flux)
OD	57.15 mm
HT	15.24 mm x 2 (two cores stacked together)
ID	26.39 mm
μ	60
Turns	20
Wire Diameter	>2.60 mm
Strand	1
Peak Current	65A
RMS Current	46A
Peak-to-Peak Ripple	5A
Frequency	140 kHz
Full Load Inductance	70 μ H
Core Loss	5.3W
Copper Loss	15.2W
Winding Factor	20%
Finished OD	58 mm
Finished HT	(2) x 16.1 mm

2.5 INPUT PROTECTION CIRCUITRY

The evaluation board protects the circuitry against input overcurrent, input inrush current and input overvoltage. The simplified schematic in [Figure 2-6](#) and component location diagram in [Figure 2-7](#) show the locations of these components.

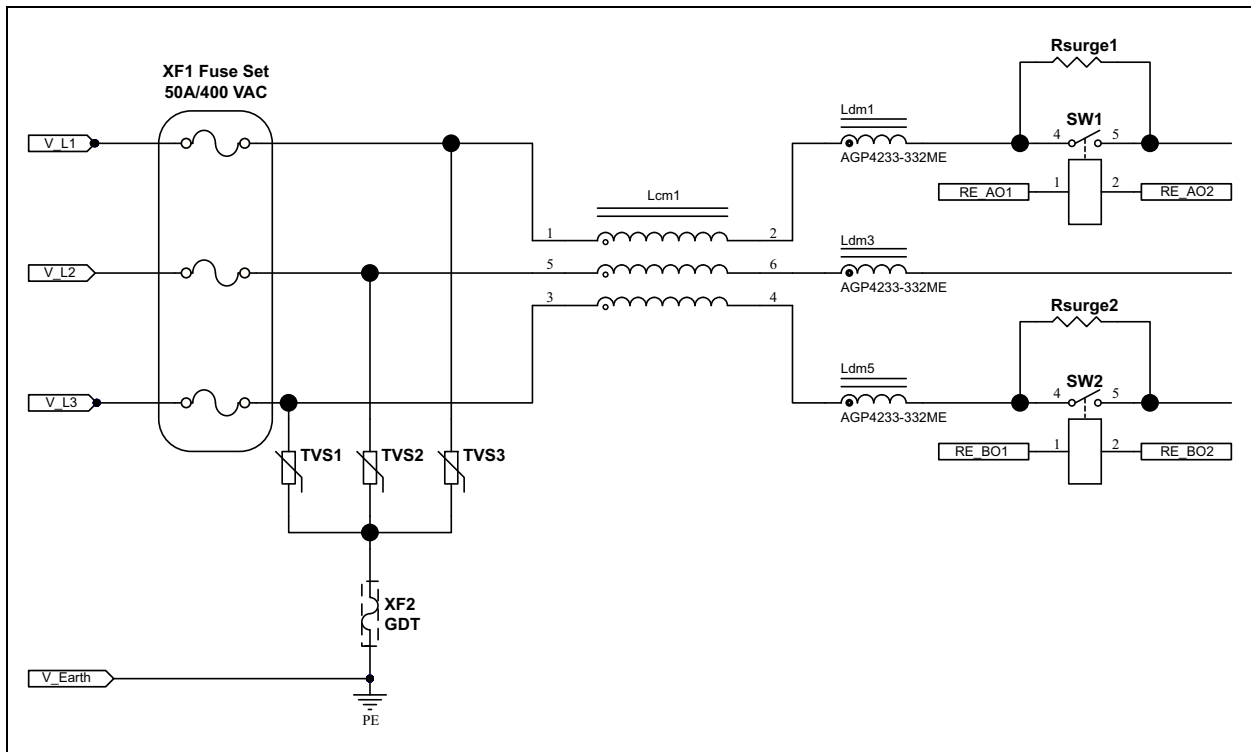


FIGURE 2-6: Input Protection Simplified Schematic.

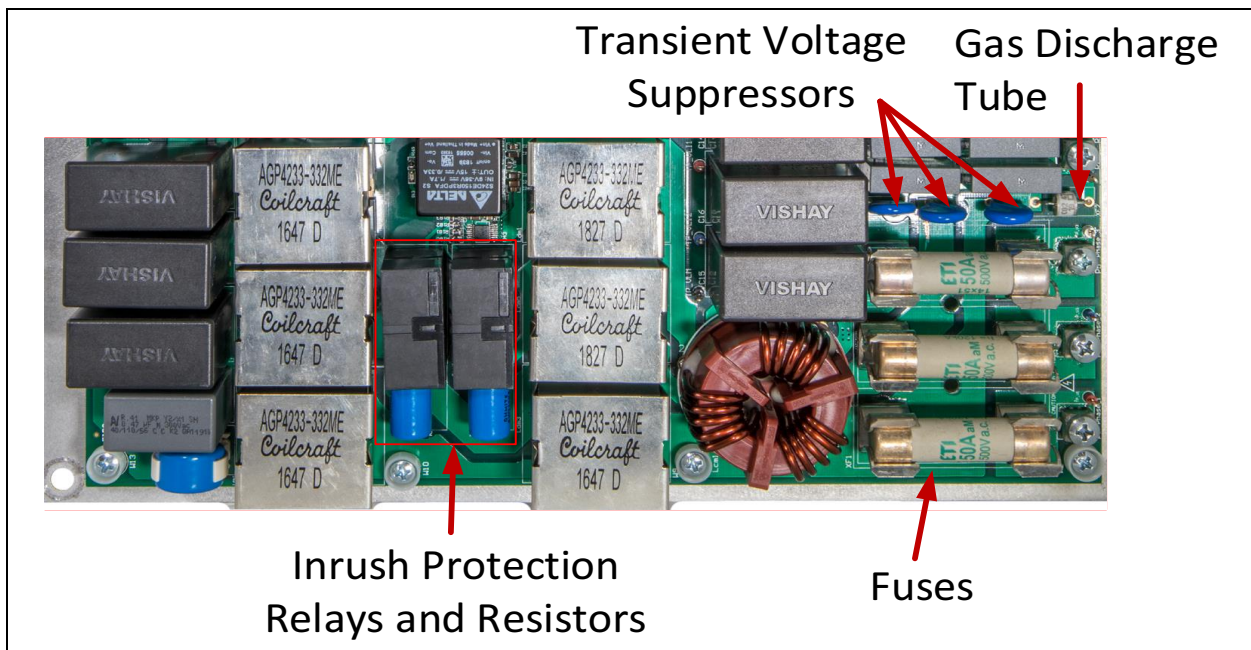


FIGURE 2-7: Input Protection Component Locations.

3-Phase 30 kW Vienna PFC Reference Design

2.5.1 Short-Circuit Protection

The input of each phase is fused to protect the board from high-current overload and short-circuit conditions.

2.5.2 Input Overvoltage Protection

A transient input overvoltage is clamped using a series combination of Metal Oxide Varistor (MOV) and a Gas Discharge Tube (GDT). The MOV breaks down at a preset voltage and will maintain that voltage until the input surge is removed. The GDT breaks down at a preset voltage, but the voltage across the tube drops to a much lower level once it begins to conduct. The advantage of this combination is a higher initial breakdown voltage to prevent false triggering and lower power dissipation during the surge event.

2.5.3 AC Mains Dropout/Brown-out

The output (DC bus) voltage will decrease during a short-term temporary loss of the AC input voltage. When the input voltage is reapplied, there will be a surge of input current until the bus voltage comes back to regulation. This time period may be too short for the relay/resistor inrush current limit circuit to respond. To prevent possible component damage and false circuit breaker triggering, the peak input current is monitored and input current is limited by the controller if it exceeds a maximum value.

Brown-out is a condition where the AC input RMS voltage drops below the normal range. During brown-out, the input current will increase to maintain delivery of a constant output power. The input current sensing circuitry will limit the maximum input current to prevent excessive input current and possible component damage. During current limit, the output voltage will drop below the regulated DC output voltage level. Once the brown-out condition goes away, the DC bus voltage will return to its regulated value.

2.5.4 Input Phase Loss

The power supply is designed to operate when all three input voltage phases are present. It will not operate during a loss of input voltage phase.

2.6 CONDUCTED EMI INPUT FILTER

The EMI filter is used to suppress both Common-mode (CM) and Differential-mode (DM) noise. The filter is comprised of two Common-mode and two Differential-mode sections. The components are selected to filter out frequencies in the 150 kHz to 30 MHz range. The input filter schematic is shown in [Figure 2-9](#) and the filter components are identified in [Figure 2-8](#).

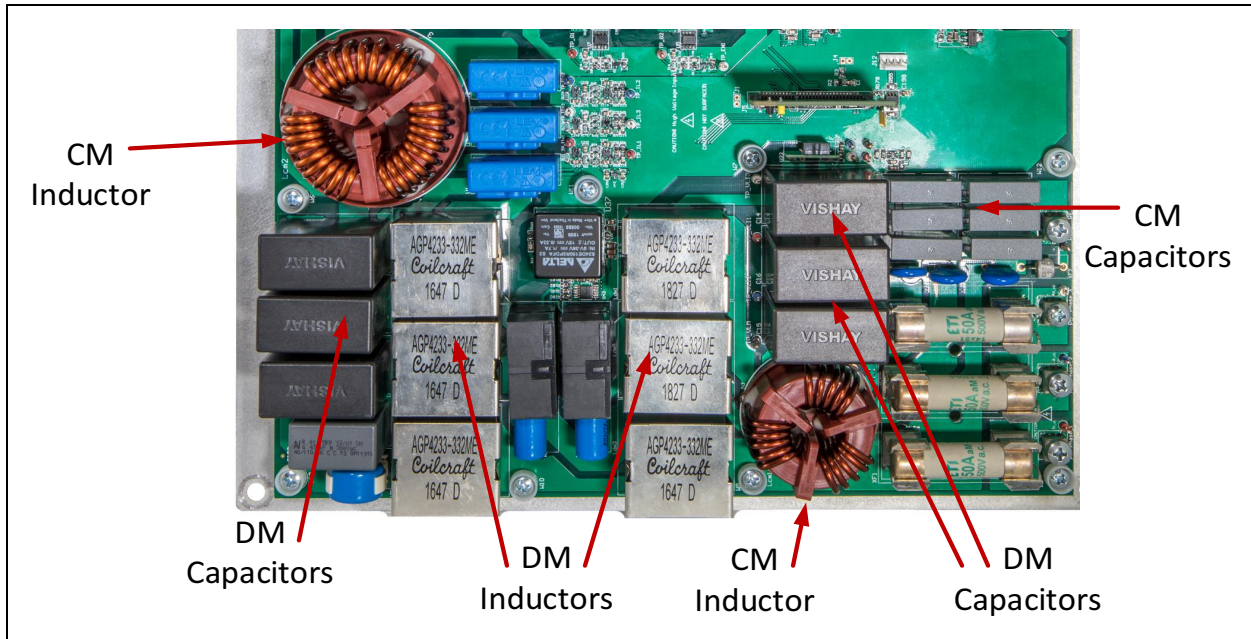


FIGURE 2-8: EMI Filter Components.

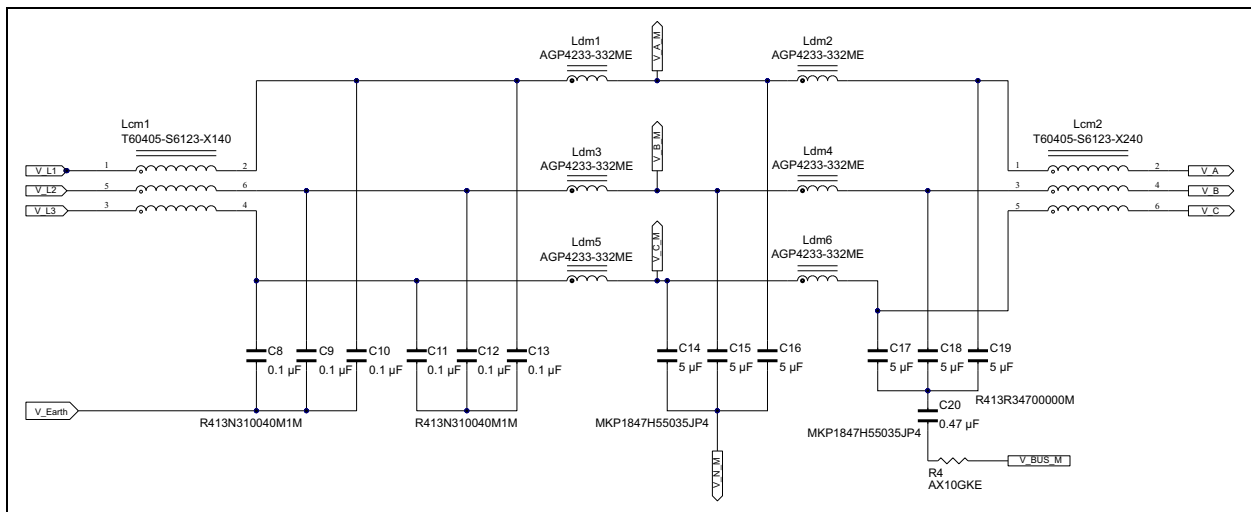


FIGURE 2-9: Input EMI Filter.

Common-mode inductor Lcm1 and capacitors, C8, C9 and C10, form a CM filter that attenuates Common-mode signals at the input. The capacitors shunt the high-frequency noise to earth ground. Note that due to the inherent properties of a 3-phase system, the line frequency leakage current into earth ground is zero.

A two-stage LC Differential-mode filter is comprised of inductors Ldm1-6 and capacitors C11-19. These components attenuate the switching frequency ripple voltage from the Vienna PFC stage. They also attenuate the higher frequency noise and ringing generated by parasitic resonances within the power supply. The capacitors are connected in a delta configuration, which minimizes the voltage stress on each component.

In addition to DM filtering, capacitors C14-16 form a virtual neutral point that is used as a reference for measuring the line neutral voltage of the input (V_N_M). Capacitor C20 connects to the output filter capacitor midpoint and provides a bypass path away from earth ground for high-frequency Common-mode noise.

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2.7 CURRENT SENSING

The current in each of the three phases is monitored by a Hall effect sensor. The current signal is processed by a pair of op amps that buffer, level shift and filter the Hall effect sensor output. The current sensing circuit for one of the phases is shown in [Figure 2-10](#).

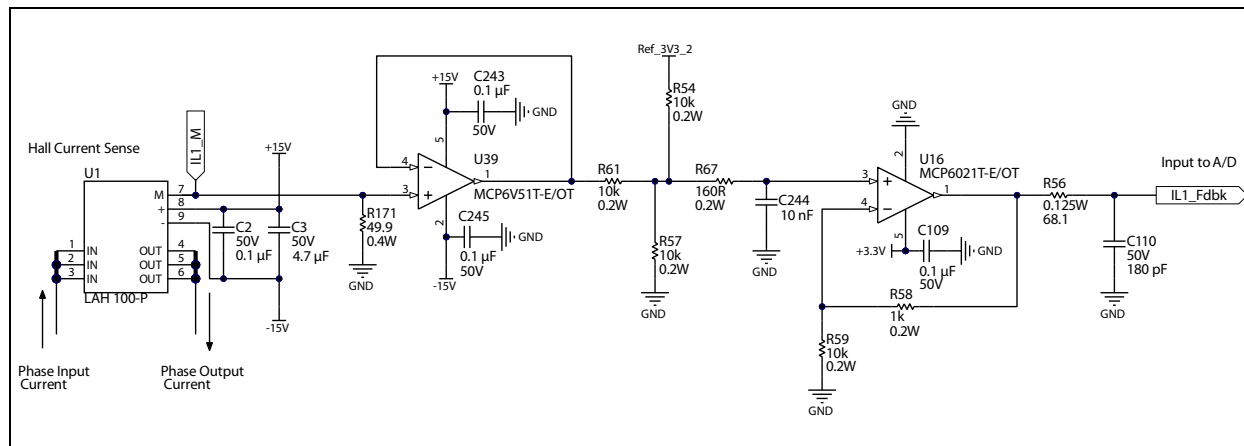


FIGURE 2-10: Current Sense Amplifier.

2.7.1 Hall Effect Sensor

The Hall effect device generates a galvanically isolated current that is proportional to the AC input current. This isolated current can either be positive or negative, which allows the device to sense current over the entire AC input cycle.

The ratio of AC input to isolated output current is 1:2000. This current flows through resistor R171 (50Ω) and generates a voltage at the input of the noninverting buffer (U39). A 100A peak-peak input current will generate a 2.5V peak-peak voltage across R171.

2.7.2 Level Shifting, Attenuation and Filtering

Positive and negative bias supply voltages allow the first op amp in the current amplifier circuit to properly buffer the bipolar current signal from the Hall effect sensor. Its output feeds three resistors (R54, R67 and R61) that level shift and attenuate the signal. For the values shown in the schematic, attenuation is 0.333 and the voltage level is shifted by +1.1V. This ensures the input voltage to the second stage op amp is always positive for the operating current range of the Vienna power stage.

Next a low-pass RC filter removes switching frequency ripple and other noise. The cutoff frequency calculation is shown in [Equation 2-12](#). For the schematic values, $f_c \sim 4.6$ kHz.

EQUATION 2-12: CUTOFF FREQUENCY CALCULATION

$$f_c = \frac{1}{2\pi \times C244 \times R_{eq}}$$

Where:

$$R_{eq} = R54 \parallel R61 \parallel R57 + R67$$

The second op amp buffers the filtered signal (with a small gain) and a high-frequency, low-pass RC filter cleans up the signal before being digitized by the A/D Converter in the MCU. The voltage gain of this op amp is 1.1 and the low-pass filter cutoff frequency is calculated by [Equation 2-13](#).

EQUATION 2-13: LOW-PASS FILTER CUTOFF FREQUENCY

$$f_c = \frac{1}{2\pi \times C110 \times R56}$$

For 180 pF and 68.1Ω, $f_c = 13$ MHz.

The overall current amplifier frequency response is shown in [Figure 2-11](#) and includes the frequency response of the two op amps.

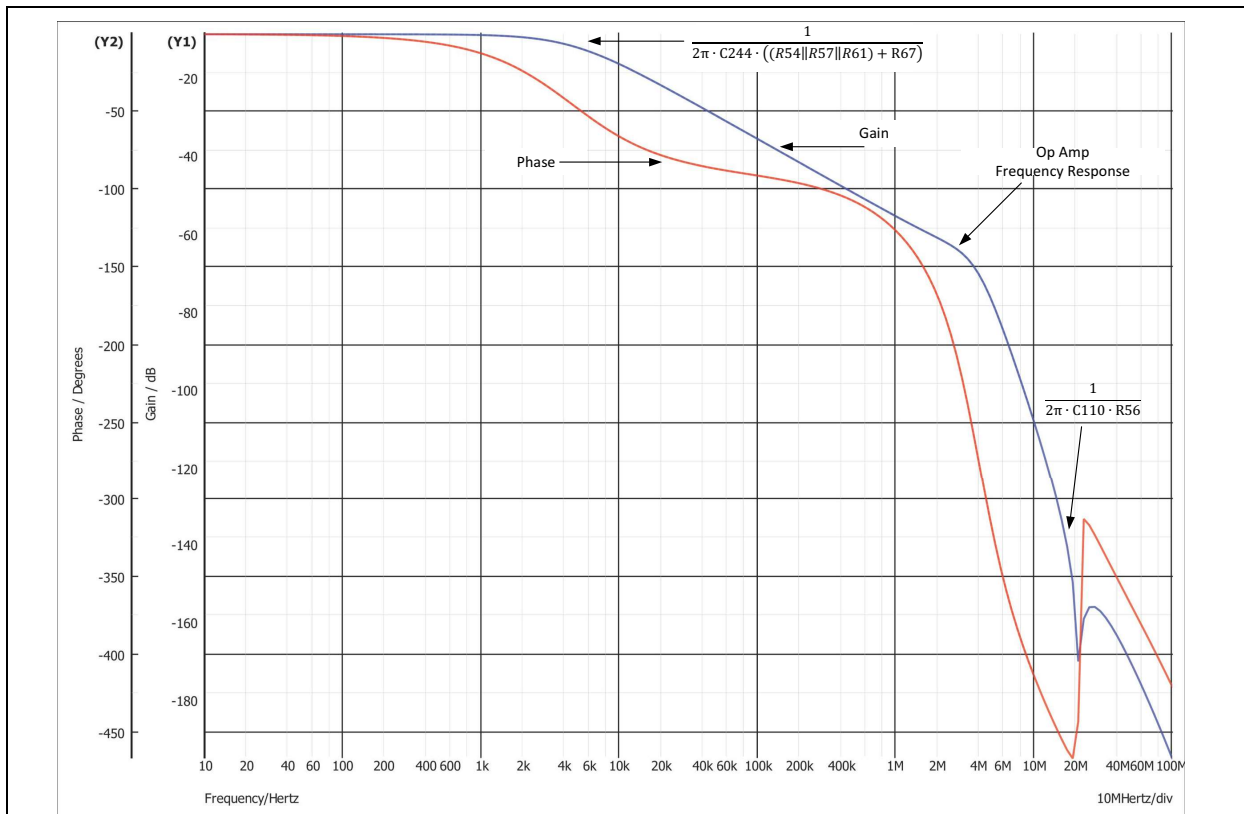


FIGURE 2-11: Current Amplifier Frequency Response.

2.8 VOLTAGE SENSING

The AC input voltages and DC output voltage are sensed using isolation amplifiers. Isolation is needed to overcome the Common-mode range, as well as safety requirements and CM noise reduction. Each of the amplifiers requires a separate isolated bias voltage.

2.8.1 AC Input Voltage Sensing

To achieve high-power factor and low harmonics, the AC input current is forced to match the AC input voltage. Isolation amplifiers are used to measure the AC input voltage for all three phases. The voltage is scaled down, isolated, filtered, then digitized by the A/D Converter in the microcontroller.

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Each of the three phases are measured, from phase to neutral, using a virtual neutral point (described in [Section 2.6 “Conducted EMI Input Filter”](#)). The maximum voltage at the isolation amplifier’s input is 250 mV. The voltage divider between phase and neutral is set up to keep the peak voltage at the isolation amplifier’s input below the 250 mV limit.

The peak line to neutral voltage is calculated from the RMS line to line voltage using [Equation 2-14](#).

EQUATION 2-14: PEAK LINE TO NEUTRAL VOLTAGE

$$V_{pk_LN} = \frac{\sqrt{2}}{\sqrt{3}} \times V_{rms_LL}$$

Referring to [Figure 2-12](#), the voltage divider is comprised on resistors, R72, R73, R75 and R78. The input impedance of the isolation amplifier (V_{INP} to V_{INN}) is approximately 18 k Ω . The input impedance is in parallel with R78 and must be included in the calculation. The peak voltage at the isolation amplifier input (V_{pk_amp}) is calculated using [Equation 2-15](#).

EQUATION 2-15: PEAK VOLTAGE AT ISOLATION AMPLIFIER INPUT

$$V_{pk_amp} = V_{pk_LN} \times \frac{R78 \parallel 18k\Omega}{R78 \parallel 18k\Omega + R72 + R73 + R75}$$

For a 400 V_{RMS_LL} input voltage, the peak voltage at the isolation amplifier input is 196 mV. The actual value is about 8% less due to the amplifier’s input pin bias currents.

Resistor R82 is needed to balance input voltage offset that is caused by DC bias current at the input pins and should be equal to R78.

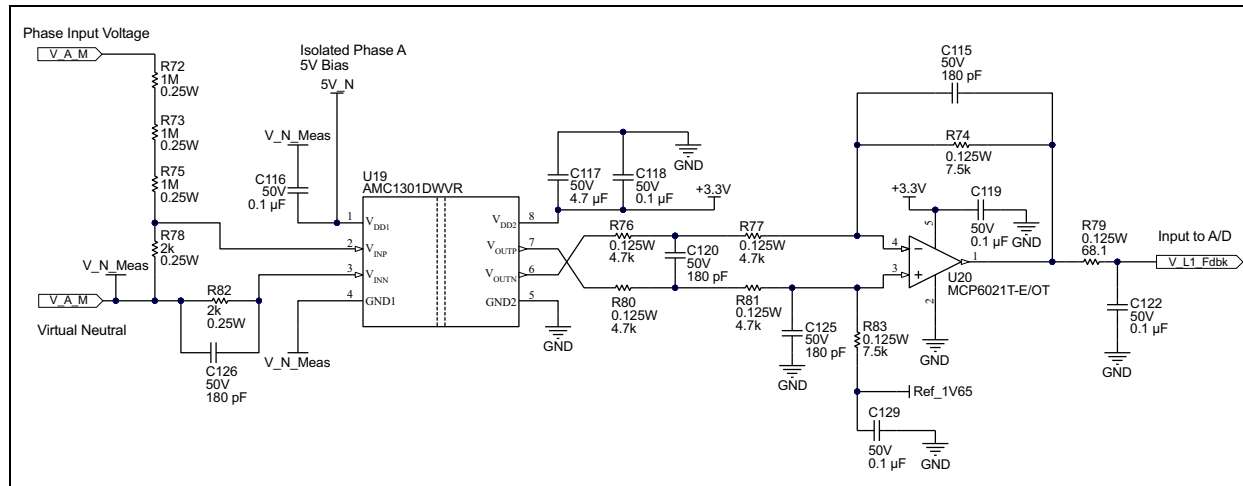


FIGURE 2-12: AC Input Voltage Isolation Amplifier.

The isolation amplifier has a gain of 8.2V/V, a bandwidth of 200 kHz and a 1.44 V_{DC} Common-mode offset at the output. The differential amplifier circuit removes the 1.44V offset, applies a gain of 0.8V/V, a positive offset of 1.65V and filters the signal with a three-pole R/C low-pass filter. When $R74 = R83$, $R76 = R80$ and $R77 = R81$, the differential amplifier DC gain and the three-pole frequencies (using the schematic values) are:

EQUATION 2-16: AMPLIFIER DC GAIN

$$G = \frac{R83}{R80 + R81} = 0.798$$

EQUATION 2-17: POLE FREQUENCY – 1

$$f_{p1} = \frac{1}{2\pi \times C120 \times 2 \times (R80 \parallel R81)} = 188kHz$$

EQUATION 2-18: POLE FREQUENCY – 2

$$f_{p2} = \frac{1}{2\pi \times C125 \times R83} = 118kHz$$

EQUATION 2-19: POLE FREQUENCY – 3

$$f_{p3} = \frac{1}{2\pi \times C122 \times R79} = 23.4kHz$$

2.8.2 DC Output Voltage Sensing

In the Vienna PFC topology, the DC output voltage capacitors are split and the SiC MOSFET connections are made to the output capacitor voltage midpoint. The high-side and low-side capacitor voltages must be monitored separately for output voltage regulation and capacitor voltage balancing.

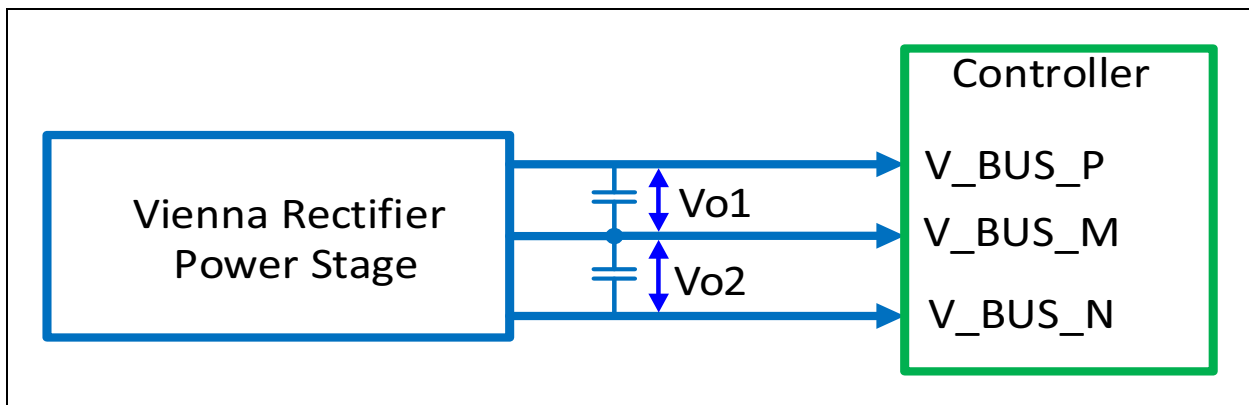


FIGURE 2-13: Split Output Voltage Capacitors.

The DC output voltage sensing circuit is shown in [Figure 2-13](#). The figure shows the upper voltage sense circuit, which connects between the DC output bus and the midpoint. The second voltage sense circuit is identical and connects between the midpoint and DC bus return. The circuit topology and operation are very similar to the AC input voltage sensing circuit with the following exceptions:

1. The output voltage divider ratio is adjusted for the DC output voltage.
2. There is no need for a Common-mode offset voltage adjustment since the DC output voltage is always positive with respect to ground.

The gain and pole frequencies are calculated using the same formulas as the AC sensing circuit. The two circuits use the same differential amplifier and filter component values with the exception that there is no 1.65V offset added to the voltage amplifier output.

EQUATION 2-20: ISOLATION AMPLIFIER INPUT VOLTAGE

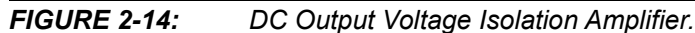
For a 700V output voltage and the schematic values shown, the amplifier input voltage is 277 mV.

The amplifier gain is calculated using Equation 2-21.

$$G_{amp3} = \frac{R110}{(R113 + R112)}$$

For the 700V DC output voltage, the output voltage of the DC amplifier circuit is calculated with Equation 2-22. The actual value is about 8% less due to the amplifier's input pin bias currents.

$$V_{BusPM_{Fdbk}} = 277mV \times 8.2 \times 0.8 = 1.81V$$



2.9 ISOLATED GATE BIAS AND DRIVE CIRCUITRY

The power stage SiC MOSFETs are connected in series with a common source, as shown in [Figure 2-15](#). Two sets of these SiC MOSFETs in parallel are required for the power level of this evaluation board. In this configuration, the SiC MOSFETs must be driven with isolated drivers. In addition to being isolated, the SiC MOSFETs are driven with a bipolar gate drive voltage of +20V/-5V. The schematic in [Figure 2-16](#) shows the isolated bias supply circuit used to generate the bipolar supply voltages with respect to isolated ground, GND1.

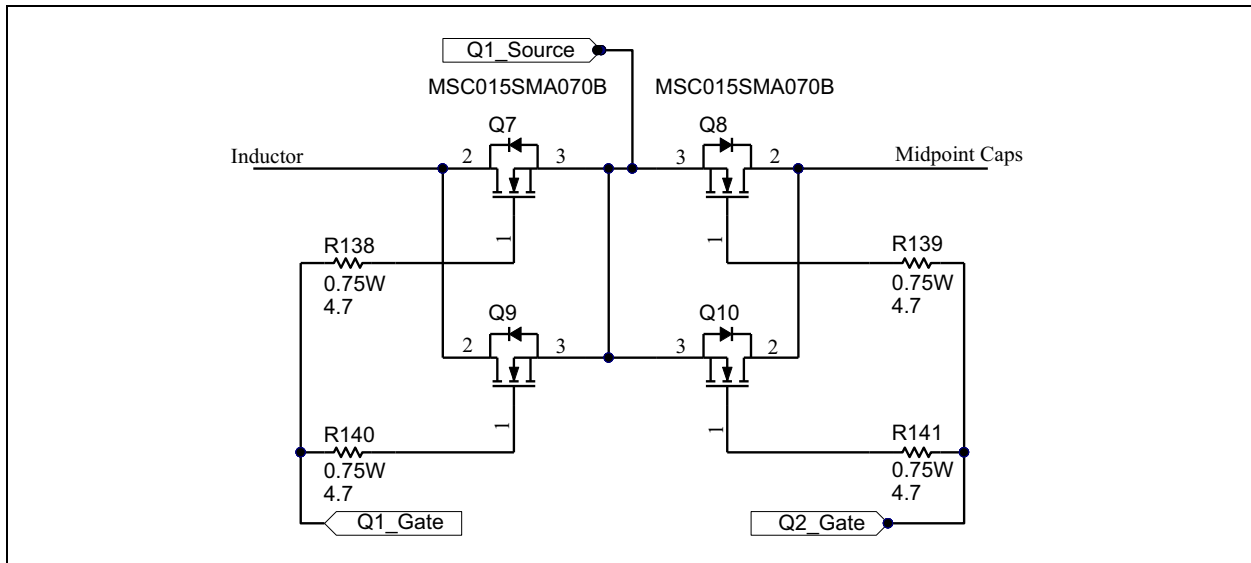


FIGURE 2-15: Switching SiC MOSFET Configuration.

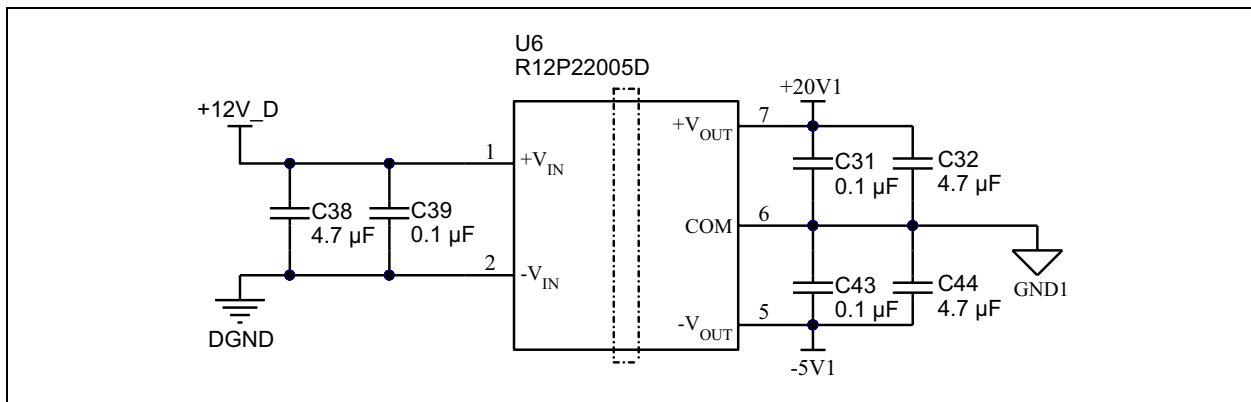


FIGURE 2-16: Gate Drive Bias Supply.

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The isolated gate driver schematic is shown in [Figure 2-17](#). A gate drive signal from the dsPIC DSC is used as an input on the low-voltage side of the driver. The signal propagates across the isolation barrier to the high-voltage side, which is biased by the +20V/-5V supply voltages. The gate drive signal is connected to the SiC MOSFET Q7/Q9. The source of Q7/Q9 is connected to the isolated ground, GND1, which is also the common point for the isolated bias supply.

When the input to the gate driver is high, the OUTH pin of the gate driver IC is pulled up to +20V (with respect to GND1/Q1_Source) and when the gate driver input is low, the OUTL pin pulls the SiC MOSFET's gate down to -5V.

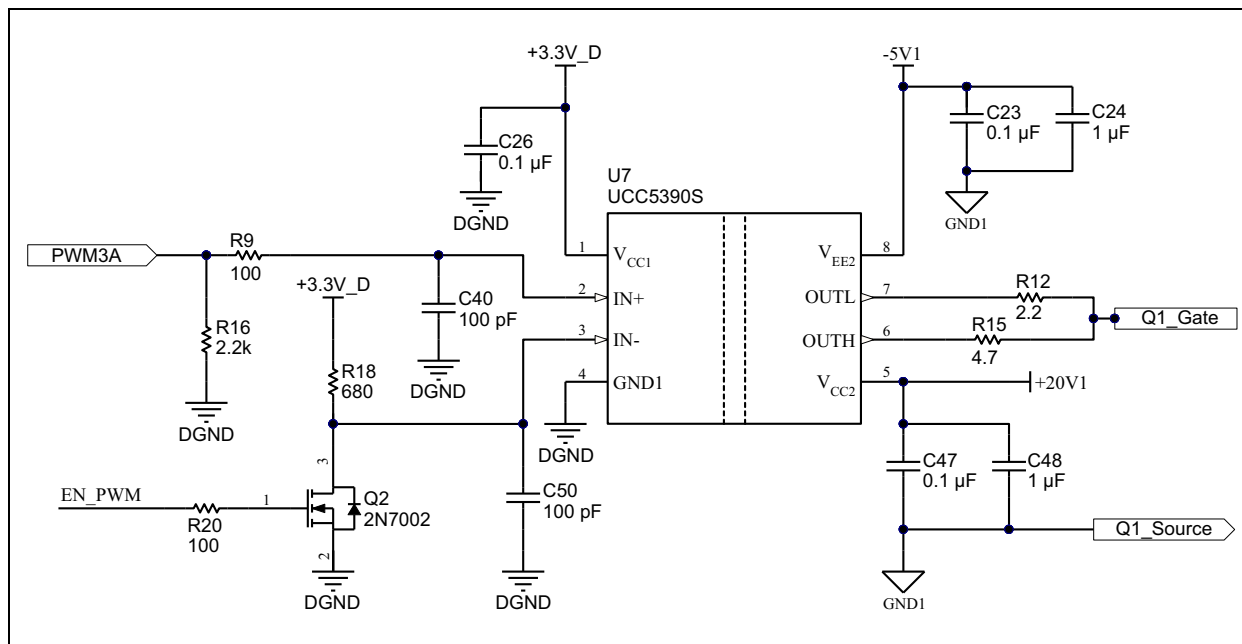


FIGURE 2-17: Isolated Gate Driver.

2.10 BIAS SUPPLIES

The evaluation board requires an external 12V supply for biasing all the internal components. The block diagram in [Figure 2-18](#) illustrates the bias power supply architecture of the evaluation board. The dotted line through some of the blocks indicates functional and/or safety isolation. The ground symbol for each block shows which ground the output is referenced to.

The external 12V input supply is isolated and regulated by a self-contained and isolated power module. Its output feeds the following circuits:

- $\pm 15\text{V}$ Isolated Supply: Bias voltages for the three Hall effect current sensors and the 1st stage of their respective current amplifier/filter circuits.
- Six $+20\text{V}/-5\text{V}$ Isolated Supplies: Each one is the bias supply for the six isolated output gate driver circuits.
- 5V Bias Supply: Supply voltage for the controller board, 3.3V supplies, references, and the isolated AC input and DC output voltage sensing circuitry.

Please refer to the schematics in the separate documentation package for detailed information.

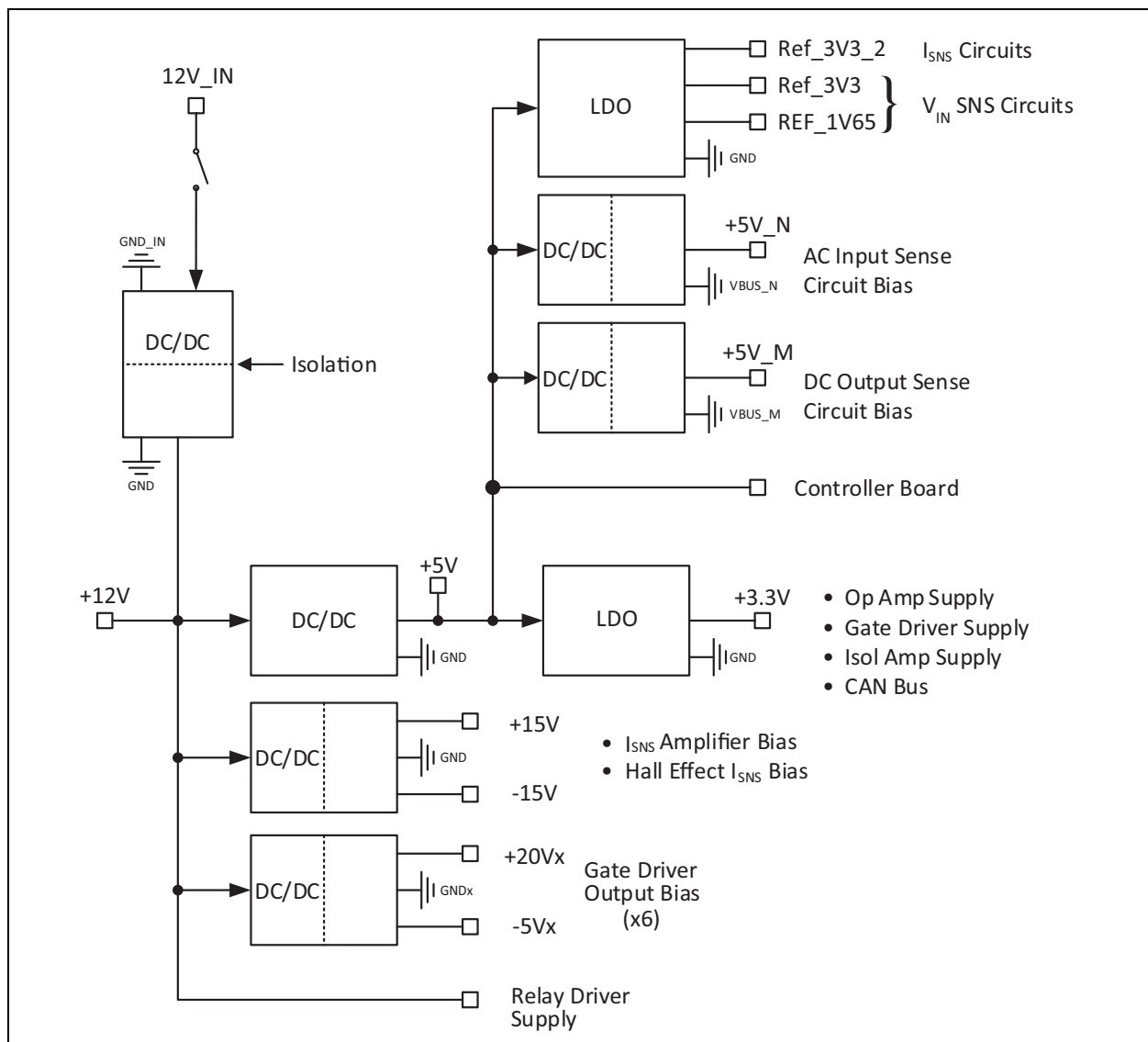


FIGURE 2-18: *Bias System Block Diagram.*

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2.11 START-UP PROCESS

A two-step start-up process is used to limit input current surges and output voltage spikes. The first part of the start-up procedure utilizes a resistor/relay scheme to limit the initial input inrush current. The second part of the start-up procedure occurs once the controller is active. It begins to modulate the switching frequency duty cycle, starting at the zero-crossing of the AC input voltage, to minimize input current and output voltage spikes. These two steps are described below.

Note: In this implementation of the software code, the inrush relays must be manually turned on and off. Please refer to [Section 1.5 “Power-up and Power-Down Procedures”](#) for the proper start-up procedure and manual operation of the inrush relays.

2.11.1 Inrush Current Limiting

The output capacitors are discharged before input voltage is applied. High-current flows from the input, through the SiC diodes, and into these capacitors when input voltage is first applied. Inrush current limiting is necessary to limit excessive and possibly damaging input current during start-up. Phase A and C each contain an inrush limiting circuit consisting of a series resistor and a bistable latching relay in parallel with the resistor, as illustrated in [Figure 2-19](#). During start-up, the relay is latched in the open state and the resistor limits the peak surge current. The relay is latched in the closed state when the peak DC output voltage increases to nearly the peak input voltage, but before the SiC MOSFETs start to switch. This prevents excessive power dissipation in the resistor. Only two of the phases require current limiting since current in the third phase (Phase B) will flow through the limiting resistors in Phases A and B.

The latching relay only requires a pulse of current to latch in the ON state. A pulse of current in the opposite direction latches the relay in the OFF state. A simple, low-power, full-bridge motor driver IC serves as a buffer between the MCU signal and the relay coil.

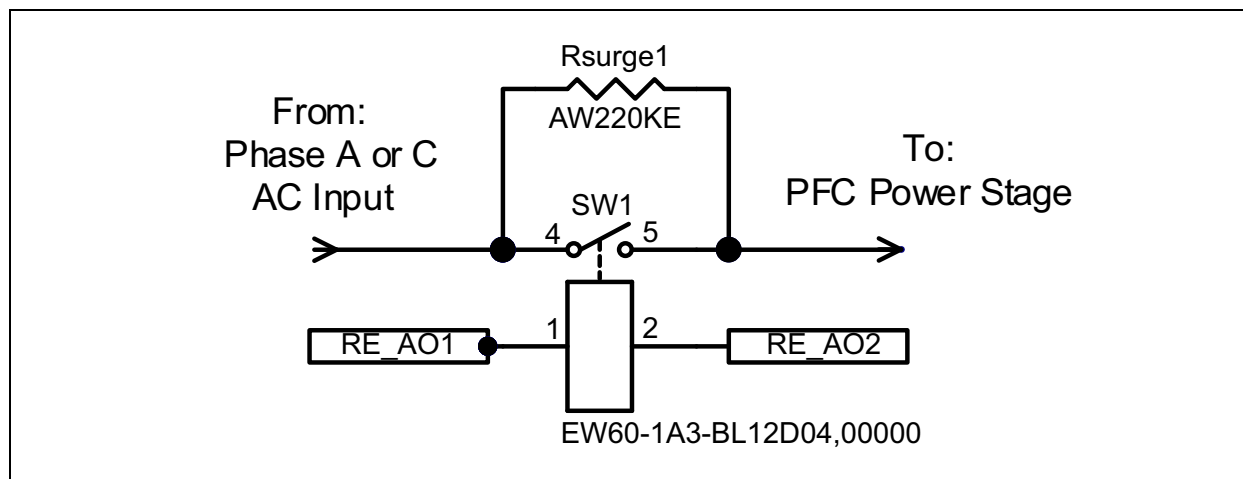


FIGURE 2-19: Inrush Relay Circuit.

The scope waveforms in [Figure 2-20](#) illustrate the first part of the start-up process.

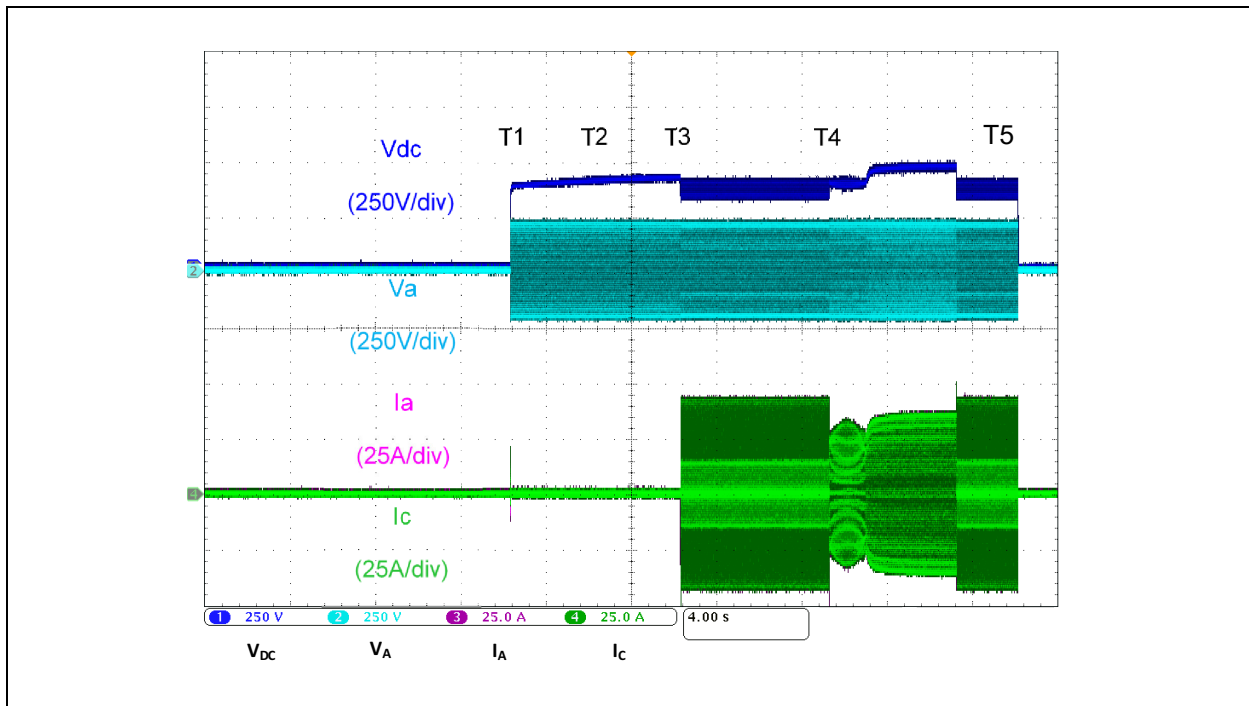


FIGURE 2-20: Inrush Protection.

At time T1, AC voltage is applied equally to all three phases. Current flowing through the Schottky SiC diodes charges up the output capacitance, as seen in the blue trace labeled V_{DC} . The small spike of current on I_A and I_C is limited by the resistor, R_{surge} . At T2, the relays are manually closed, which short out the two current-limiting resistors that are in series with Phases A and C. At T3, the output load bank is connected and the input current on the three phases increases to supply the output current to the load. At T4, the control circuit drives the SiC MOSFETs, which boost up the output voltage to its regulated value and begin forcing the input current to match the input voltage. At T5, the AC voltage is removed from the power supply input.

2.11.2 Boost Start-up Process

Once the inrush relays are closed, the controller is activated and begins the process of starting up the converter. The controller works to minimize the inrush current as the switching process starts and the output voltage increases to its regulated value. It also is designed to prevent output voltage spikes during start-up. To achieve these goals, the controller:

1. Sets the voltage loop controller coefficients according to the output load before switching occurs. This allows a controlled start-up over the output load current range.
2. Begins switching the SiC MOSFETs for each phase at the zero-current crossing.
3. Applies the output voltage reference ramp to the voltage control loop after the start-up point.

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The PFC converter start-up into a constant resistance load is shown in [Figure 2-21](#). Once the SiC MOSFETs begin to switch, the peak output current is reduced because the converter is forcing an in-phase sinusoidal current instead of a pulsed input current. After a period of approximately 800 ms, the output voltage reference is ramped up and the output voltage rises to its regulated value. This is done slowly to minimize any inrush current and/or output voltage spikes.

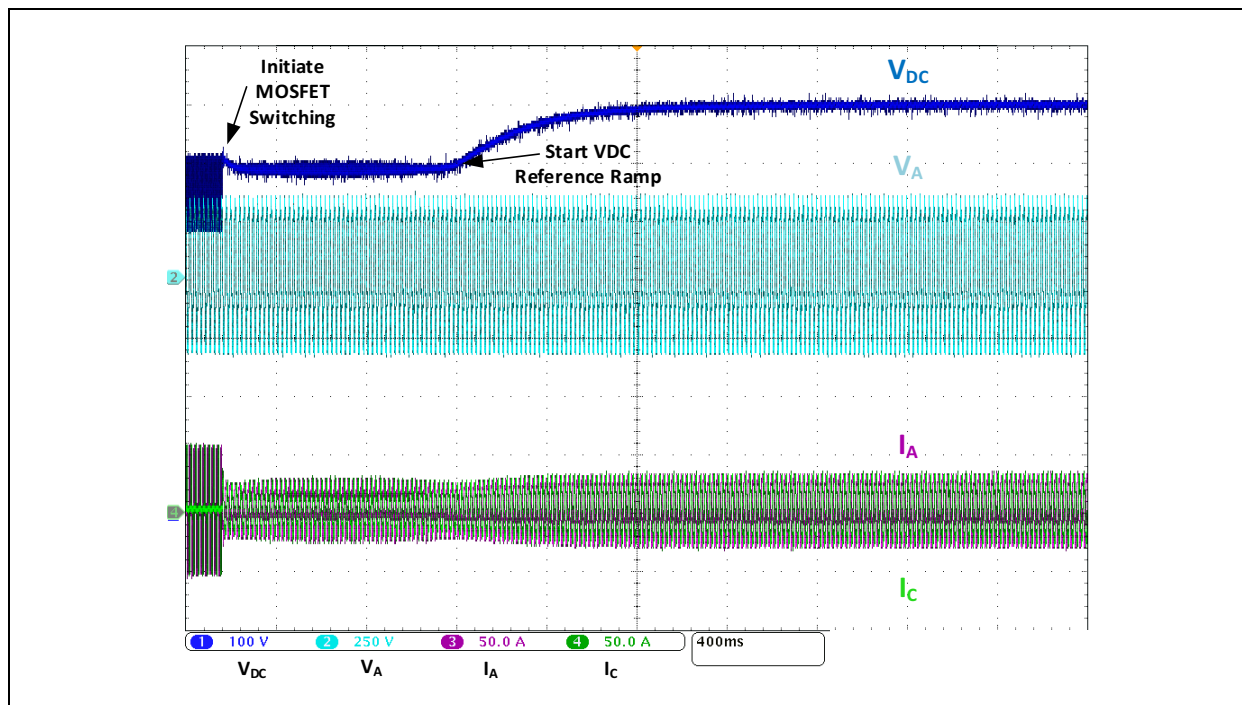


FIGURE 2-21: Start-up Process.

A closer examination of the time when the SiC MOSFETs start to switch is shown in [Figure 2-22](#). Before the SiC MOSFETs begin to switch, the input current waveforms are similar to a passive 3-phase bridge and the output voltage ripple is high due to the high peak input currents and the non-continuous current flowing into the output. The SiC MOSFETs begin to turn on when the input current is at 0 to prevent voltage and current spiking from occurring. The AC current becomes sinusoidal within a line frequency period. With 3-phase continuous sinusoidal current flowing to the output, the output voltage ripple is greatly reduced.

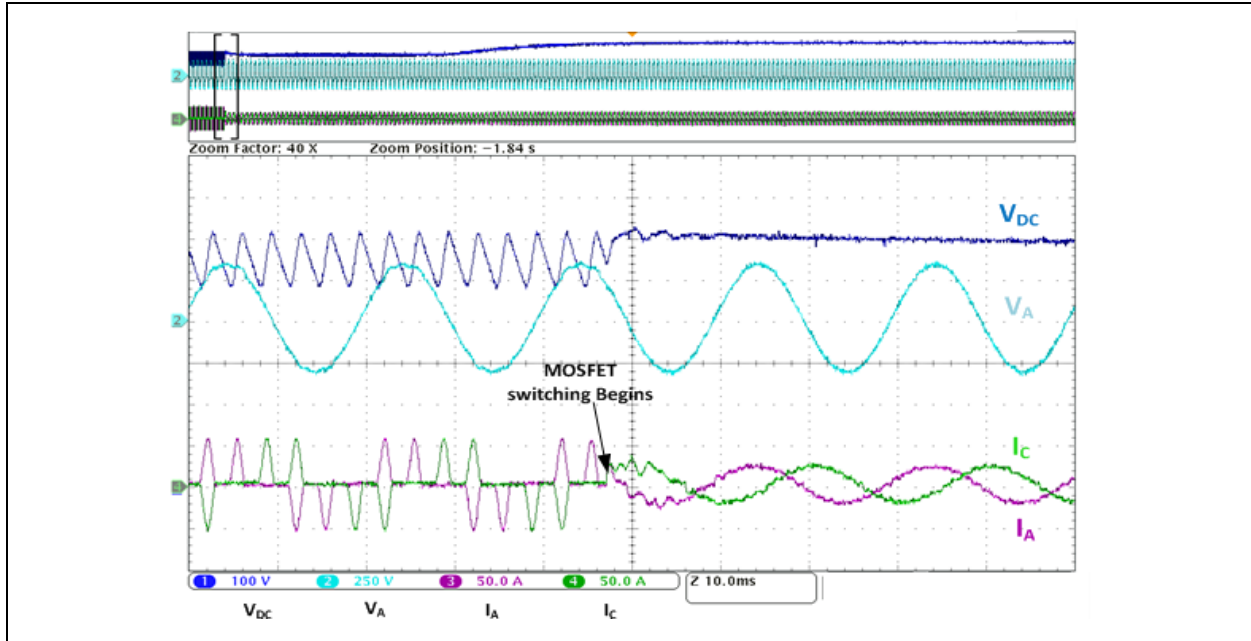


FIGURE 2-22: Beginning of the Start-up Process.

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2.12 CONTROLLER

The dsPIC33CH512MP506 dual core microcontroller is optimized for 3-phase digital control in real-time applications. The fast and high-quality 12-bit Analog-to-Digital Converter enables accurate measurement of the current and voltage signals, and the 3-phase optimized Core Independent Peripherals (CIPs) minimize CPU overhead. The high-speed CPU core enables fast execution of the voltage and current control loops. Additional information about the controller may be found at this link:

[dsPIC33CH512MP506](#).

2.12.1 Controller Functions

Figure 2-23 illustrates the control functions of the Vienna PFC. The control functions are broken up into four parts:

1. Output Voltage Control: Regulates the DC output voltage.
2. Voltage Balancing Control: Maintains equal voltage on the high and low output capacitors.
3. 3-Phase PFC Control: Forces each of the three input currents to match the shape and phase of their respective input voltages. A PI-RES control algorithm is used to minimize 5th, 7th, 11th and 13th line frequency harmonics.
4. Three-Level Modulator: Sets the power stage switching frequency and generates the continuously varying duty cycle that drives the SiC MOSFETs for each of the three phases.

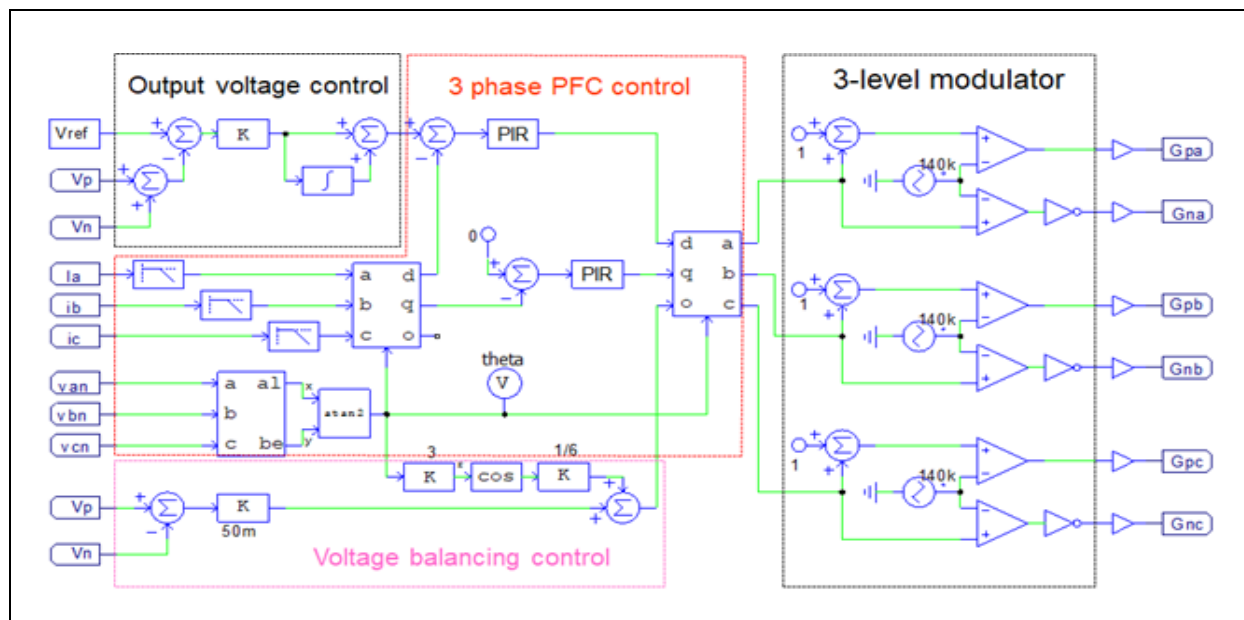


FIGURE 2-23: Control Function Block Diagram.

2.13 FIRMWARE AND DOCUMENTATION

Firmware and additional documentation can be found on the Microchip Vienna PFC Evaluation Board product page at this link: www.microchip.com/PFC.

2.14 CONNECTORS AND TEST

Table 2-2 below shows the connectors on the main power board.

TABLE 2-2: MAIN POWER BOARD CONNECTORS

Connector	Pin Number	Function	SCH Name
P1	—	Input Voltage Phase A	Vienna_PFC_Overall
P3	—	Input Voltage Phase B	
P5	—	Input Voltage Phase C	
P7	—	Input Chassis Ground	
P2	—	Output Voltage Positive	
P4	—	Output Voltage Midpoint	
P6	—	Output Voltage Negative	
J6	—	Power Supply Input 12V: Connect a 12V external power source to this connector before applying the AC input voltage	Vienna_PFC_PowerSupply
J7	—	Fan Connector	
J8	—	Fan Connector	
J9	—	Fan Connector	
J1	1	ADC-A1, DACOUT: Connection to DAC output for debugging	Vienna_PFC_Controller
J1	2	ADC-A0, DACOUT RTN: Ground	
J4	1	Remote Enable: Short to ground (Pin 2) to enable converter, open to disable	
J4	2	Remove Enable RTN: Ground	
J12	1	CAN GND	
J12	2	CAN L	
J12	3	CANH	
J12	4	CAN +3.3V	
J5	dsPIC® DSC PIM Board Connector		
J5	1, 2, 58, 60	Ground: dsPIC DSC board ground	Vienna_PFC_Controller
J5	3	DAC OUT: Analog output of dsPIC DSC DAC	
J5	5	V_L1_Fdbk: Isolated Phase A reference voltage input	
J5	9	V_L3_Fdbk: Isolated Phase C reference voltage input	
J5	11	V_L2_Fdbk: Isolated Phase B reference voltage input	

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TABLE 2-2: MAIN POWER BOARD CONNECTORS (CONTINUED)

Connector	Pin Number	Function	SCH Name
J5	12	IL1_Fdbk: Isolated Phase A current reference input	Vienna_PFC_Controller
J5	13,15	RE_IN1B, RE_IN2B: Input to relay driver for Phase C inrush limiter outputs	
J5	14	IL3_Fdbk: Isolated Phase C current reference input	
J5	16	IL2_Fdbk: Isolated Phase B current reference input	
J5	17	V_BUSPM_Fdbk: Isolated output voltage reference voltage measured from Vbus_P to V _{BUS} midpoint input	
J5	20	V_BusMN-Fdbk: Isolated output voltage reference voltage measured from V _{BUS} midpoint to Vbus_N input	
J5	24	EN_PWM: Output from dsPIC DSC to SiC MOSFET drivers; Low = All drivers disabled and all SiC FETs off; High = All drivers enabled	
J5	25	CAN RX: Receive signal from CAN transceiver	
J5	27	CAN TX: Transmit signal from CAN transceiver	
J5	31	STBY: Standby Signal to Inrush Relay Driver: A low forces all relay driver outputs to high-impedance; a high enables the outputs for operation	
J5	33,35	RE_IN1A, RE_IN2A: Input to relay driver for Phase A inrush limiter outputs	
J5	37	PWM3A: SiC MOSFET gate driver input for Phase A positive SiC MOSFETs	
J5	40	PWM2B: SiC MOSFET gate driver input for Phase B negative SiC MOSFETs	
J5	41	PWM3B: SiC MOSFET gate driver input for Phase A negative SiC MOSFETs	
J5	42	PWM2A: SiC MOSFET gate driver input for Phase B positive SiC MOSFETs	
J5	45	PWM1A: SiC MOSFET gate driver input for Phase C positive SiC MOSFETs	
J5	47	PWM1B: SiC MOSFET gate driver input for Phase C negative SiC MOSFETs	
J5	54	Button: Remote enable signal input to dsPIC DSC; Low = Enable, High = Disable	
	57,59	+5V: 5V bias supply to dsPIC DSC	
J5	4,6,7,8,10,18,19,23,26,28,29,30,32,34,36,38,39,43,44,46,48,49,50,51,52,53,55,56	dsPIC DSC PIM Board Connector: No connection	

TABLE 2-3: TEST ITEMS AND TEST PINS FOR MEASURING WAVEFORMS

Test Point	Test Item	Color	SCH Name
TP_V1	Input Voltage Phase A	Black	Vienna_PFC_EMIFilter
TP_V2	Input Voltage Phase B	Red	Vienna_PFC_EMIFilter
TP_V3	Input Voltage Phase C	Blue	Vienna_PFC_EMIFilter
TP_PE1	Input Voltage PE	White	Vienna_PFC_EMIFilter
TP_VL7	Output Voltage Positive	Red	Vienna_PFC_PowerStage
TP_N1	Output Voltage Neutral	White	Vienna_PFC_PowerStage
TP_VL8	Output Voltage Negative	Black	Vienna_PFC_PowerStage
TP_EN1	EN_PWM	Blue	Vienna_PFC_GateDriver
TP_DGND1	DGND	Black	Vienna_PFC_GateDriver
TP_G1	PWM3A	Red	Vienna_PFC_GateDriver
TP_GS1	Q1_Gate	Red	Vienna_PFC_GateDriver
TP_G2	PWM3B	White	Vienna_PFC_GateDriver
TP_GS2	Q2_Gate	White	Vienna_PFC_GateDriver
TP_G3	PWM2A	Red	Vienna_PFC_GateDriver
TP_GS3	Q3_Gate	Red	Vienna_PFC_GateDriver
TP_G4	PWM2B	White	Vienna_PFC_GateDriver
TP_GS4	Q4_Gate	White	Vienna_PFC_GateDriver
TP_G5	PWM1A	Red	Vienna_PFC_GateDriver
TP_GS5	Q5_Gate	Red	Vienna_PFC_GateDriver
TP_G6	PWM1B	White	Vienna_PFC_GateDriver
TP_GS6	Q6_Gate	White	Vienna_PFC_GateDriver
TP_GND1	Q1_Source	Black	Vienna_PFC_GateDriver
TP_GND2	Q3_Source	Black	Vienna_PFC_GateDriver
TP_GND3	Q5_Source	Black	Vienna_PFC_GateDriver
TP_IIn1	Phase A Current Input	Black	Vienna_InductorCurrentSensor
TP_IL1	Phase A Current Measured	Black	Vienna_InductorCurrentSensor
TP_IIn2	Phase B Current Input	Red	Vienna_InductorCurrentSensor
TP_IL2	Phase B Current Measured	Red	Vienna_InductorCurrentSensor
TP_IIn3	Phase C Current Input	Blue	Vienna_InductorCurrentSensor
TP_IL3	Phase C Current Measured	Blue	Vienna_InductorCurrentSensor
TP_VLI1	Phase A Voltage Input	Black	Vienna_InputVoltageSensor
TP_VL1	Phase A Voltage Measured	Black	Vienna_InputVoltageSensor
TP_VLI2	Phase B Voltage Input	Red	Vienna_InputVoltageSensor
TP_VL2	Phase B Voltage Measured	Red	Vienna_InputVoltageSensor
TP_VLI3	Phase C Voltage Input	Blue	Vienna_InputVoltageSensor
TP_VL3	Phase C Voltage Measured	Blue	Vienna_InputVoltageSensor
TP_VLM	V_N_Meas (GND)	White	Vienna_InputVoltageSensor
TP_GND	Analog Ground	White	Vienna_InputVoltageSensor
TP_VPM	V _{BUS} Positive Input	Red	Vienna_OutputVoltageSensor
TP_BUSM	V _{BUS} Neutral	White	Vienna_OutputVoltageSensor
TP_VNM	V _{BUS} Negative Input	Black	Vienna_OutputVoltageSensor
TP_VBUSPM_Fdbk1	VPM Measure	Red	Vienna_OutputVoltageSensor
TP_VBUSMN_Fdbk1	VMN Measure	Black	Vienna_OutputVoltageSensor

Chapter 3. Testing and Results

3.1 KEY WAVEFORMS

Key waveforms at full load (29 kW) are shown in [Figure 3-1](#). AC input voltage, V_A , is 400 V_{RMS}/50 Hz. Switching frequency is 140 kHz and the output voltage is 700 V_{DC}. Efficiency at full load is 98.5% and input current THD is 2.6%.

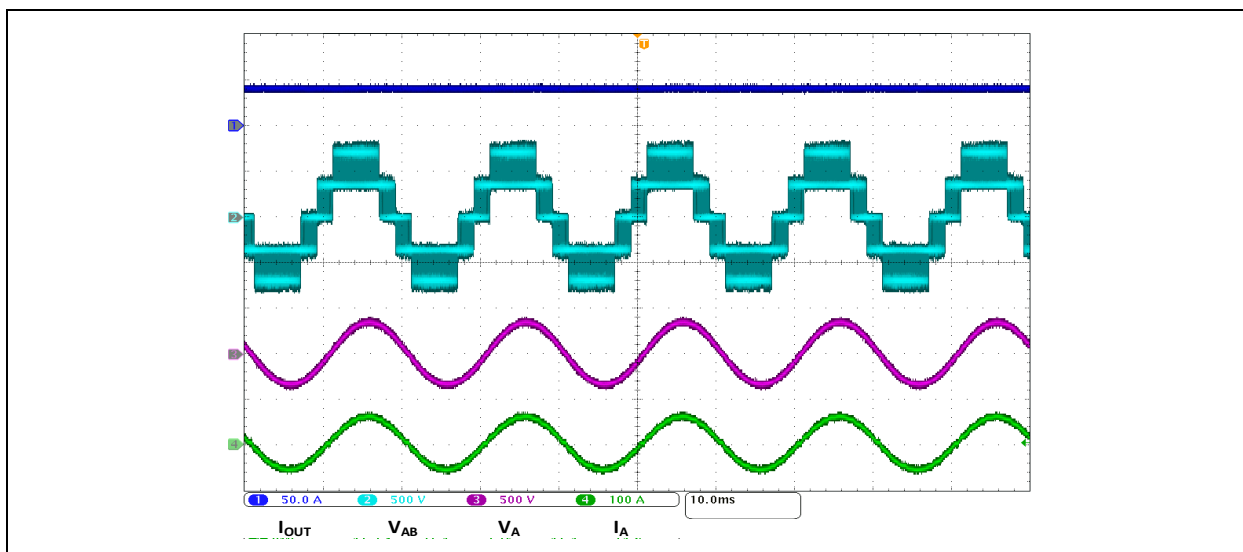


FIGURE 3-1: Steady-State Waveforms at 29 kW.

[Figure 3-2](#) shows the efficiency vs. output power, and input current THD vs. output power for $V_{IN_LL(RMS)} = 400V$, $V_{DC} = 700V$, $f_{LINE} = 50$ Hz and $f_S = 140$ kHz.

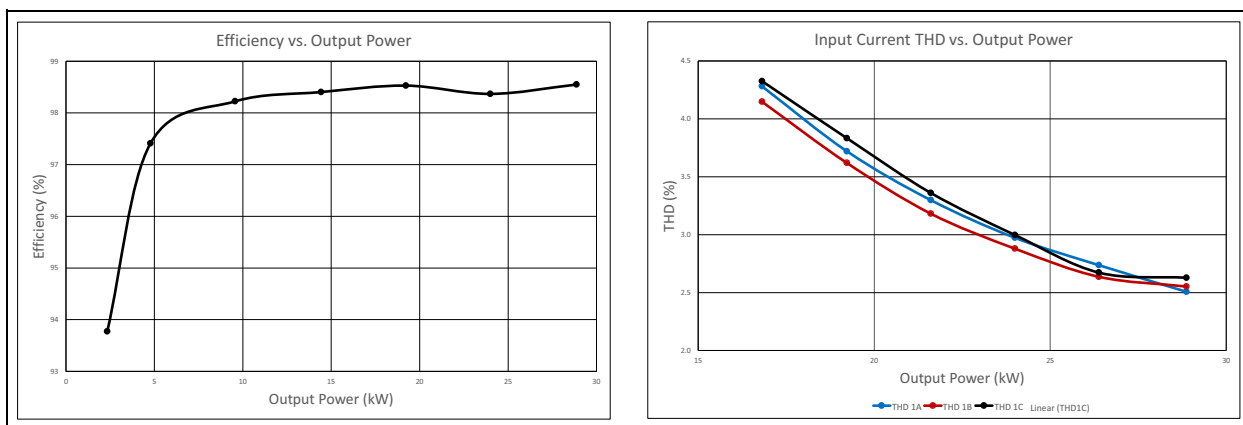


FIGURE 3-2: Efficiency and THD vs. Output Power.

Chapter 4. Thermal Design

4.1 INTRODUCTION

Heat sinking is required for the SiC MOSFETs. Each of the three phases uses a set of four SiC MOSFETs and two SiC diodes, which are attached to an extruded aluminum heat sink. The SiC MOSFET packages are isolated from the heat sink using a single sheet of AlN. A phase change thermal interface material is applied to the heat sink side of the AlN insulator and to the back side of the MOSFET packages to improve thermal conductivity. The SiC diodes are attached to the bottom of the heat sink using screws, insulating grommets and are insulated using a thermally conductive graphite insulator sheet. Please refer to the BOM for vendors and part numbers. The heat sink used is a Fischer Elektronik LAM5 K 150 12. It is a 50 mm x 50 mm x 150 mm extrusion with a high-performance cooling channel composed of internal fins. The included cooling fan is removed and replaced with a higher performance fan. Please refer to the BOM for vendor and part number information. A mechanical drawing of the heat sink is shown in [Figure 4-1](#). [Figure 4-2](#) illustrates the diodes attached to the bottom of the heat sink.

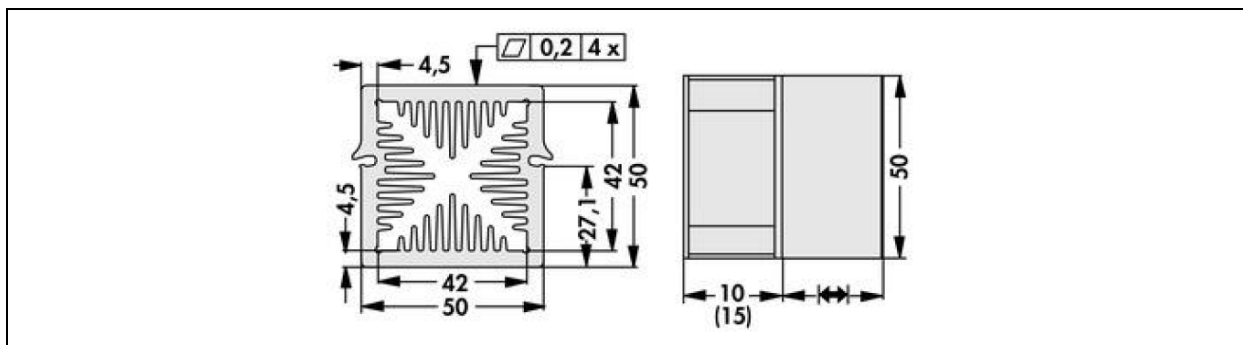


FIGURE 4-1: Heat Sink Drawing and Thermal Performance.

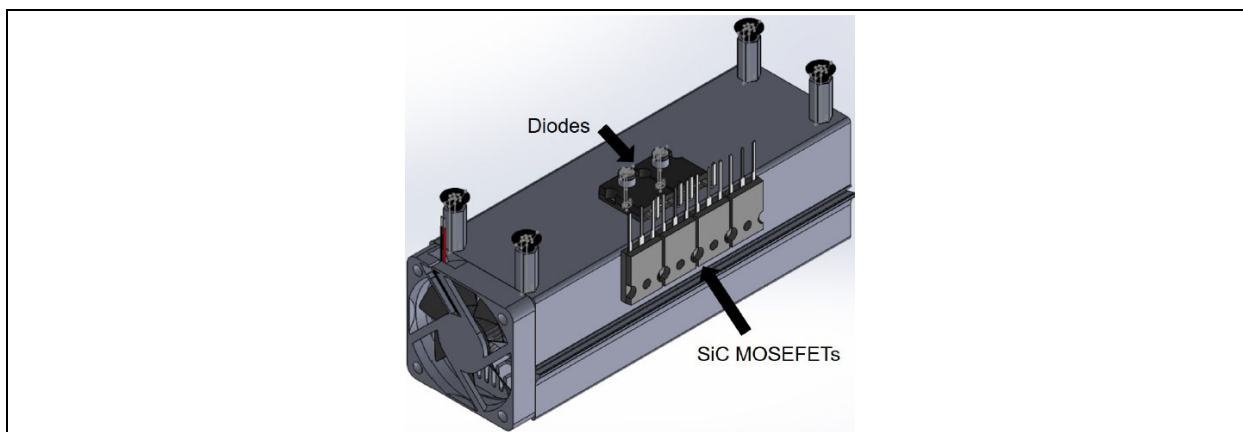


FIGURE 4-2: SiC Diode Attachment.

3-Phase 30 kW Vienna PFC Reference Design

Figure 4-3 shows the thermal performance of the heat sink for a 400 VAC input and 27 kW output power. Maximum case temperature of the SiC MOSFET is ~80°C.

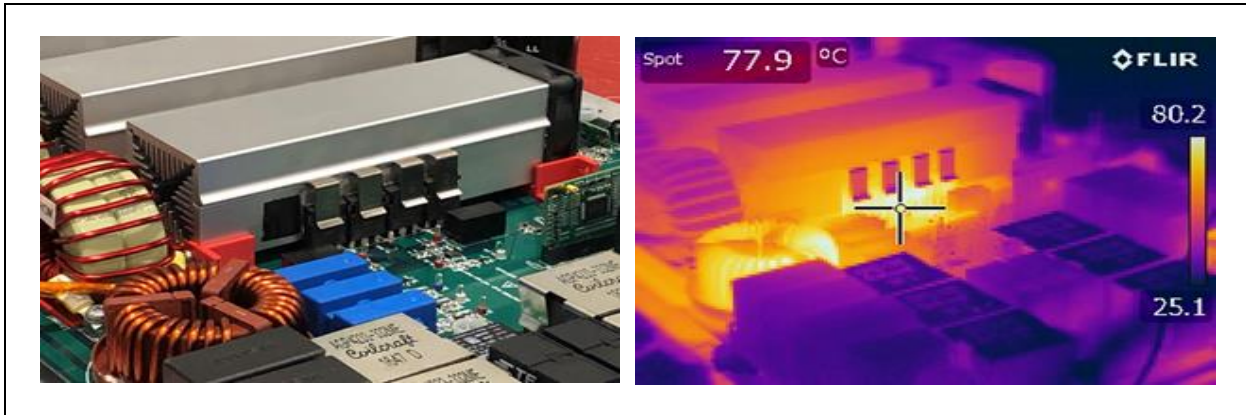


FIGURE 4-3: Heat Sink and SiC MOSFET Temperature.

Chapter 5. Mechanical Design and Assembly

5.1 INTRODUCTION

This section describes some of the mechanical aspects of how the evaluation board is assembled. Please note that some of these brackets and methods of attachment were designed for this evaluation board and may not be suitable for production units.

5.2 MECHANICAL ASSEMBLY

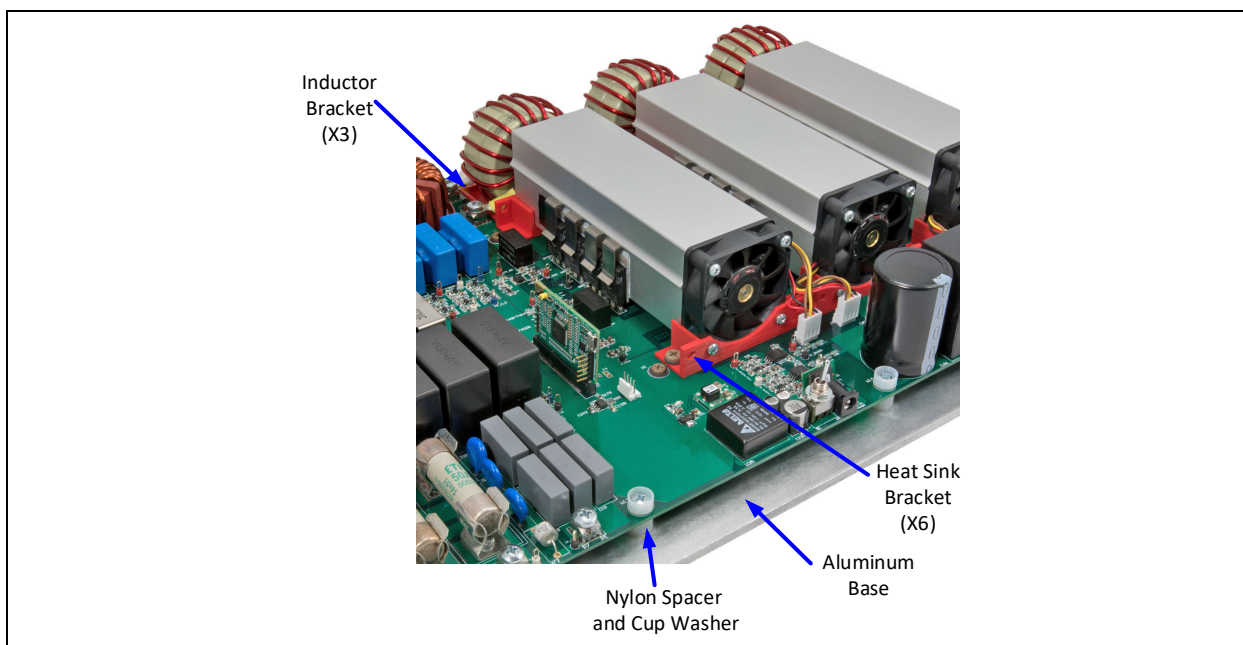


FIGURE 5-1: Mechanical Board and Heat Sink Assembly.

The board is mounted on a rigid aluminum base to prevent flexing and damage when lifting or transporting. For safety reasons, the base must be earth grounded when AC input voltage is applied to the board and it is operating. The nylon spacers and cup washers provide adequate insulation, and spacing for test and evaluation purposes, but may not meet all of the safety agency requirements.

Metal screws are used to attach the board to the aluminum base and to make electrical connections. There are some brackets and parts that use plastic screws to prevent short-circuit or arcing issues between components and high-voltage PCB traces. These plastic screws may not be suitable for environments with high shock and vibration.

3-Phase 30 kW Vienna PFC Reference Design

Figure 5-2 and Figure 5-3 illustrate how board stiffeners are used under the heat sinks due to the weight in that area of the board.

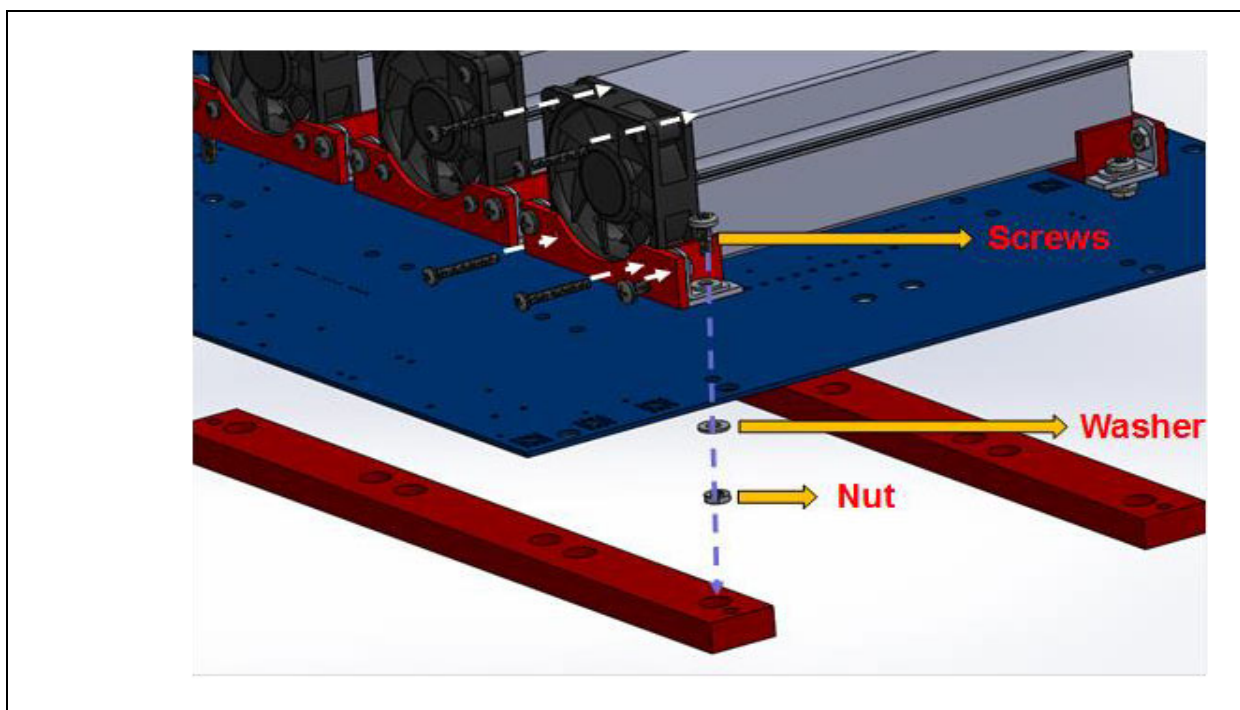


FIGURE 5-2: Heat Sink to PCB Assembly Diagram.

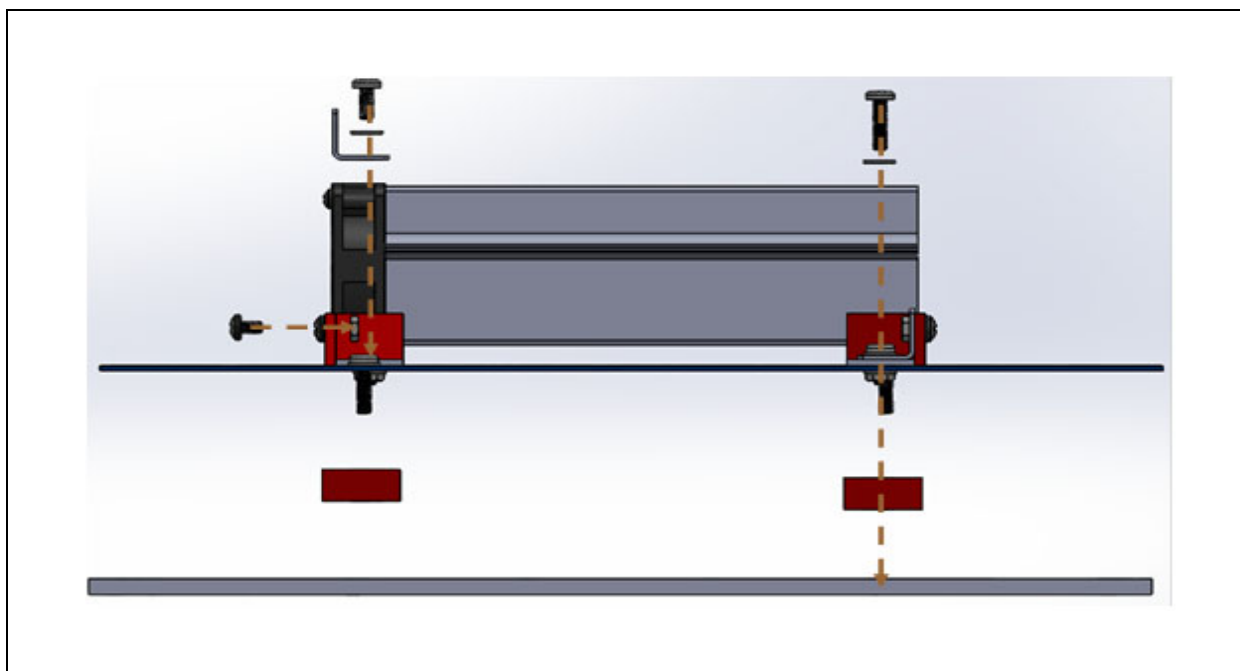


FIGURE 5-3: Heat Sink to PCB Assembly – Side View.

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