



MICROCHIP

PD69200/PD69210/PD69220/PD69200M
Firmware 3.54 Release Notes

1. General

- **Affected Part Numbers:** PD69200/PD69210/PD69220/PD69200M
- **Distinction:** According to package label, software version read from the device.
- **Effective Date:** February 16, 2021

2. Introduction

The following release note describes firmware release (3.54), which is to be used on Microchip PD692x0 devices. PD692x0 Version 3.54 controller supports the following Microchip PoE devices:

- PD39208
- PD69208M
- PD69208T4
- PD69204T4

See *PD692x0 Serial Communication Protocol User Guide version 3.30* for more information.

To load a new firmware version into an existing PD692x0 device, use the UART/I²C interface, follow the 'Firmware Download' procedure.

3. New Features

3.1. Add support in PD39208

Add support in mix system with PD69208 and PD39208.

The PD39208 supports only 2 pair matrix, with power limitation of 630mA / 32Watt.
(POE10XX-159).

3.2. New feature – Reserved Power

User can allocate power to a port or few ports, before or after the ports are turned-on.

The allocated power is taken from the main power budget, and used only for the ports set to reserved-power.

Two new commands were added in 3.54 in order to support reserved-power:

- Set BT Port Reserved Power Request
- Get BT Port Reserved Power Request

Also, a new port operational mode was added to set the port to reserved power, mode 0x31.

Please refer to **PD692x0 Serial Communication Protocol User Guide version 3.30** for more information.

Set BT Port Reserved Power Request

| [0] KEY | [1] ECHO | [2] SUB | [3] SUB1 | [4] SUB2 | [5] DATA | [6] DATA | [7] DATA | [8] DATA | [9] DATA | [10] DATA | [11] DATA | [12] DATA |
|------------|-------------|------------|----------------|-------------|------------------------|-------------|---------------|-------------|-------------|--------------|--------------|--------------|
| 0x00 | ## | 0x05 | 0x55 | Val | Val | | Val | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E |
| Command | | Channel | Reserved Power | Port Num | Reserved Power Request | | PSE Port Type | N | N | N | N | N |

Get BT Port Reserved Power Request

| [0] KEY | [1] ECHO | [2] SUB | [3] SUB1 | [4] SUB2 | [5] DATA | [6] DATA | [7] DATA | [8] DATA | [9] DATA | [10] DATA | [11] DATA | [12] DATA |
|------------|-------------|------------------------|----------------|------------------------------------|-------------|-----------------|-------------|---------------|-------------|--------------|--------------|--------------|
| 0x02 | ## | 0x05 | 0x55 | Val | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E |
| Request | | Channel | Reserved Power | Port Num | N | N | N | N | N | N | N | N |
| 0x03 | ## | Val | | Val | | Val | Val | Val | 0x4E | 0x4E | 0x4E | 0x4E |
| Telemetry | | Reserved Power Request | | Reserved Power Allocated (TPPL_BT) | | Reserved Status | Priority | PSE Port Type | N | N | N | N |

| | | |
|------|--|---|
| 0x31 | 4P BT Reserved power, up to 97.5w + Legacy Detection (4P Matrix) | <p>This mode is Type4 BT up to 97.5w using reserved power configuration only.</p> <p>Note: When the mode is set, the default reserved power before power configuration is 0w.</p> <p>Maximum Logical Port Power = 97.5w</p> <p>Legacy Detection = Enable (Legacy detected PD will be treated as SSPD).</p> <p>PD69208M device will be clamped by ICUT/ILIM</p> <p>Default ICUT and ILIM are set according to the PSE Port Type and the M/T4 device bit.</p> |
| | 2P BT Reserved power, up to 48.7w + Legacy Detection (2P Matrix) | <p>This mode is Type3 BT up to 48.7w using reserved power configuration only.</p> <p>Note: When the mode is set, the default reserved power before power configuration is 0w.</p> <p>Maximum Logical Port Power = 48.7w (with TPPL clamping function)</p> <p>Legacy Detection = Enable (Legacy detected PD will be treated as SSPD).</p> <p>PD69208M device will be clamped by ICUT/ILIM</p> <p>Default ICUT and ILIM are set according to the PSE Port Type and the M/T4 device bit.</p> |

(POE10XX-158).

3.3. New port operational mode which set the port to IEEE802.3at mode.

This mode is intended to 100% pass “PSE Conformance Test”.

This mode supports only 2 pair up to 30W.

| | | |
|------|-----------------------------|--|
| 0x09 | 4P as 2P-AT 30w (4P Matrix) | <p>This mode is Type2 AT/AF compliant up to 30w with class-based power, delivers power over 2P-Primary only.</p> <p><u>The generated number of fingers is class dependent:</u></p> <p>Classes 0 to 3 = Single narrow class event + Mark till power up.</p> <p>Class 4 = 2x narrow class events that must report identical class value.</p> <p><u>Class power is per PD Type:</u></p> <p>Classes 0 to 3 will be treated as requested class 3 = 15w (Type 1), Class4 = 30w (Type2).</p> <p>Demotion is not supported.</p> <p>Maximum Logical port Power = 30w</p> <p>Legacy Detection = Disable</p> <p>Note:</p> <p>Primary pair-set must be valid detected and Secondary pair-set must be valid detected or open (Other values will be considered as logical port detection failure with no powering).</p> <p>All PDs are treated as SSPD.</p> |
|------|-----------------------------|--|

| | | |
|--|--------------------------|---|
| | 2P AT 30w (2P Matrix) | <p>This mode is Type2 AT/AF compliant up to 30w with class-based power.</p> <p><u>The generated number of fingers is class dependent:</u></p> <p>Classes 0 to 3 = 1 narrow class event, Class 4 = 2x narrow class events that must report identical class.</p> <p><u>Class power is per PD Type:</u></p> <p>Classes 0 to 3 will be treated as requested class 3 = 15w (Type 1), Class4 = 30w (Type2).</p> <p>Demotion is not supported. Maximum Logical port Power = 30w Legacy Detection = Disable</p> |
|--|--------------------------|---|

(POE10XX-165).

3.4. Improvement in Class 5 added power

The maximum “added power” in class 5 was changed from 2.5Watt to 3.7Watt.

Therefore, a class 5 dual signature PD (DSPD), can be set up to 97.5Watt.

(POE10XX-161).

3.5. Features removal / Code reduction

In order to reduce the size of the firmware, the following features were removed from version 3.54:

1. Derating feature with all related protocol commands.
2. VOP drift management feature with it's relevant save structure. This may have implications on systems using older PD69208 Revision V2R2 (LD). Note an End of Life (EOL) PCN for PD69208 Revision V2R2 (LD) was issued November 1, 2017. Please contact Microchip for details.

(POE10XX-143).

4. Bugs Fix

4.1. Bug Description: Wrong status of disconnection in 4 pair port

These 2 issues were related to wrong status report of 4 pair port.
(POE10XX-153/152).

4.2. Bug Description: PD69220, pin 29 was set wrongly

Pin 29 was set to be an output low instead to input with internal pull-up.
(POE10XX-160).

4.3. Bug Description: Disable event on a port in middle of class can cause CPU reset

When port was disabled during the first phase of the class process, a wrong class message was sent to the class module causing the PD692x0 to reset it-self.
(POE10XX-167).

4.4. Bug Description: Wrong report of connection check in CDP mode

When DSPD load was connected to a PSE port that was configured to operation mode 0x22 (CDP) the connection check result was wrongly SSPD.
(POE10XX-166).

4.5. Bug Description: Demoted SSPD port, configured with wrong power limitation

When SSPD load with high class (for example class 5) port is demoted to a lower class due to operation mode limitation, it needs to be powered up in a staggered sequence.
In this case, the lcut/llim of the primary pairset were configured with incorrect values.
(POE10XX-162).

4.6. Bug Description: In some cases, UDL event was not updated the counter

When the unbalanced algorithm detected a UDL event and generated the UDL event for the logical port, the UDL event of the logical port didn't raise and the UDL counter didn't incremented.
(POE10XX-157).

4.7. Bug Description: Factory default bit is not updated as expected

The factory default bit in the “Get BT system status” command didn’t always report correctly when system is set to default configuration.
(POE10XX-155).

4.8. Bug Description: PD692x0 might reset itself when disabling all ports.

The issue occurs when connecting multiple SSPD 4pair loads to a system with 12 PD69208/4. When all logical ports are delivering with SSPD loads and a disable all ports command is initiated, then the CPU may reset itself due to internal watchdog event.
(POE10XX-154).

5. Known Bugs/Limitations

5.1. **“Get BT Port Class” returns wrong values after programming a new matrix, and defined ports set to undefined with the new matrix**

Undefined port (Alt A & Alt B set to 0xFF) should return 0 Watt in requested power, but the value returned by the firmware is above 0 Watt.

To avoid such issue, the user should not execute the command for undefined ports.

(POE10XX-20)

5.2. **DSPD port is limited to 60W in LLDP commands, in certain condition.**

When DSPD is connected to the port, Mask 0x2C functions as it is set to 1, even it is set to 0.

(POE10XX-144)

5.3. **When port is set to type 4, and the PD is removed from the port port by the user, the port might report as OVT.**

This limitation is actual only in type 4 ports setting and might be seen once a while.

6. Collateral

- a) *All features and commands are described in the PD692x0 Communication Protocol user guide version 3.30, and “PD69200M Shared Memory Protocol” version 4.00 (PD69200M only).*
- b) *PD69208T4/PD69204T4/PD69208MPoE PSE Manager Datasheet - DS00003428*
- c) *PD69210/PD69220 PoE PSE Controller Datasheet - DS00003424*
- d) *PD69200 PoE PSE Controller Datasheet - DS00003460*
- e) *PD-IM-7604-4M/T4 EVB User guide - Document number PD-000354473*
- f) *PD-IM-7608-2 EVB User Guide - Document number PD-000303240*

7. Ordering Options

To order PoE controller programmed with 3.54 firmware, please mark "PD692x0R-035400" in the purchase order.

x: Controller P/N (i.e PD69200, PD69210, PD69220)

Example:

- PD69210R-035400 is PD69210 pre programmed with firmware 3.54 (R: Detection Method = IEEE802.3at/bt compliant PD's only)

8. Default parameters setting version 3.54

This section describes the default configuration.

8.1 General Parameters

- Ports enable/disable – Enable
- Ports type – Type 4 (90Watt)
- Ports 2 pair/4 pair – 4 pair
- Private label - 0x00
- User Byte – 0xFF

8.2 Power Parameters

- Power Banks:
 - Bank 0= 2000W
 - Bank 1= 2000W
 - Bank 2= 2000W
 - Bank 3= 2000W
 - Bank 4= 2000W
 - Bank 5= 2000W
 - Bank 6= 2000W
 - Bank 7= 2000W
 - Bank 8= 2000W
 - Bank 9= 2000W
 - Bank 10= 2000W
 - Bank 11= 2000W
 - Bank 12= 2000W
 - Bank 13= 2000W
 - Bank 14= 2000W
 - Bank 15= 2000W
- Vmin=48
- Vmax=58.5
- Power Indication LED: 82-85% for percentage mode, 32-34 Watts for power mode.

8.3 IC Status

TSH (Temperature Alarm): The upper temperature alarm limit per PoE device - 110°C

8.4 Interrupt

All interrupt events are masked (not generating interrupt signal).

8.5 Matrix

- 4 pairs 48-ports system
- Each logic port is constructed by two PD69208x physical ports.

| Logic port | Physical A | Physical B |
|------------|------------|------------|
| 0 | 0 | 8 |
| 1 | 1 | 9 |
| 2 | 2 | 10 |
| 3 | 3 | 11 |
| 4 | 4 | 12 |
| .. | .. | .. |
| 47 | 87 | 95 |

8.6 Ports Priority

All ports are set to Low (Priority =3).

8.7 Class Power limit

- Class 0 - 16.4W
- Class 1 – 5W
- Class 2 – 8W
- Class 3 - 16.4W
- Class 4 AF – 16.4W
- Class 4 AT – 33W
- Max Port Power AT – 33W

8.8 BT Port Parameters:

- CFG1= 0x01 (Port Enable)
- CFG2= 0x01 (Port TPPL_BT)
- Port Operation Mode 0x00 (90W 4P, 30W 2P, no legacy)
- Add power for port mode = 0Watt
- Priority: Low
- BT Class Additional Power = 0Watt
- Maximum power user can add to BT class additional power:
 - Class [1] = 2.5 Watt
 - Class [2] = 2.5 Watt
 - Class [3] = 3.1 Watt
 - Class [4] = 8.0 Watt
 - Class [5] = 3.7 Watt
 - Class [6] = 5.0 Watt
 - Class [7] = 7.0 Watt
 - Class [8] = 7.5 Watt

8.9 Individual Mask

| Number | Name | Value |
|--------|--|-------|
| 0x00 | Ignore higher priority | 1 |
| 0x10 | Support High res detection | 0 |
| 0x14 | Hardware reset on ASIC error | 1 |
| 0x1B | I ² C restart enable | 1 |
| 0x1F | PSE powering PSE checking | 1 |
| 0x20 | Led Stream Type | 0 |
| 0x2A | Enable ASIC Refresh | 0 |
| 0x2C | Layer2 Power Allocation Limit | 1 |
| 0x30 | Blinks in Connection check Error & Invalid Sig | 1 |
| 0x32 | Temperature Derating enable | N.A |
| 0x33 | Temperature Derating Negative\Positive Delta | N.A |
| 0x40 | xSystem OK pin behavior | 0 |
| 0x46 | Single detection fail event | 0 |
| 0x49 | Auto Zone2 port activation | N.A |
| 0x4F | Adding half priority for LLDP ports | 1 |
| 0x50 | HOCPP - High Over Current Pulse Protection | 2 |
| 0x53 | LER – Long Error Recovery | 0 |

Identifying the assembled PoE Controller

9. Identifying the assembled PoE Controller

This document is valid to all 4 PoE controllers: PD69200, PD69210, PD69220, PD69200M.

In order to identify which PoE controller is assembled, please execute the command "Get Software Version", as described in section 4.1.19 of the **PD692x0 Communication Protocol User Guide**.

The response from the PoE controller includes the **Prod#**, which indicates the PoE controller type.

Please refer to the PoE controller type list below.

4.1.19 Get Software Version

| [0] KEY | [1] ECHO | [2] SUB | [3] SUB1 | [4] SUB2 | [5] DATA | [6] DATA | [7] DATA | [8] DATA | [9] DATA | [10] DATA | [11] DATA | [12] DATA |
|------------|-------------|---------------|-------------|---------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|
| 0x02 | ## | 0x07 | 0x1E | 0x21 | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E | 0x4E |
| Request | | Global | Versionz | SW Version | N | N | N | N | N | N | N | N |
| 0x03 | ## | Val | 0x4E | Val | Val | | Val | Val | Val | | Val | |
| Telemetry | | HW Version | N | Prod# | SW_Version | | Param# | Build# | Internal SW# | | 0x0000 | |

| Prod# (Decimal) | PoE Controller Type |
|--------------------|--|
| 22 | PD69200 Programed with IEEE802.3at Firmware |
| 24 | PD69200 Programed with IEEE802.3bt Firmware |
| 27 | PD69210 Programed with IEEE802.3at Firmware |
| 26 | PD69210 Programed with IEEE802.3bt Firmware |
| 28 | PD69220 Programed with IEEE802.3at Firmware |
| 29 | PD69220 Programed with IEEE802.3bt Firmware |
| 23 | PD69200M Programed with IEEE802.3at Firmware |
| 25 | PD69200M Programed with IEEE802.3bt Firmware |

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