



Micrel KSZ8463 Switch Application Notes

Rev 1.0

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1 Revision History

Revision	Date	Summary of Changes
1.0	06/06/11	Initial revision.

2 Introduction

This document describes how to use Micrel KSZ8463 switch in software. The switch is used in the KSZ8463MLL and KSZ8462HLL chips. The software implementation is done in a Linux driver. The driver uses sysfs to provide an interface so that users can access the switch without using any application.

Each section describes a feature in the switch. Inside the section is **Register Description** where registers related to the feature are displayed. They are copied from the KSZ8463 datasheet. Refer to that datasheet for more information.

After **Register Description** is **Sysfs Variables** where variables related to the feature are described. The sysfs variables are attached to the device created by the driver. For a network devices they are located in the directory `/sys/class/net/eth?`. For a SPI devices they are located in the directory `/sys/bus/spi/devices/spi?`.

The main global variables are located under the subdirectory `sw`. Variables from each switch port is located under the subdirectory `sw[port]` where `[port]` is 0, 1, or 2. Because of the way the sysfs variables is implemented in the driver, all variables under a port subdirectory is preceded with `[#]_` where `[#]` is the same as the port number.

The switch has a static MAC address table with 8 entries. The variables used for the table are located under the subdirectory `mac[index]` where `[index]` is 0 to 7. All variables under that subdirectory are also preceded with `[#]_` where `[#]` is the same as the index.

The switch has a VLAN table with 16 entries. The variables used for the table are located under the subdirectory `vlan[index]` where `[index]` is 0 to f in hexadecimal. All variables under that subdirectory are also preceded with `[#]_` where `[#]` is the same as the index.

For those subdirectories with an index value only the maximum index is shown. In the case of switch ports it implies some variables, and so some functions, are not available in port 2, the host port.

2.1 Register Description

Chip ID Register (0x000 – 0x001)

Bit	Default	R/W	Description
15-8	0x84	RO	Family ID
7-4	0x3, 0x4	RO	Chip ID
3-1	0x0	RO	Revision ID
0	1	RW	Switch Enable

2.2 Sysfs Variables

sw/reg

The `reg` variable is used to access registers in the switch. Writing a “reg” value in hexadecimal returns the value in the register. Writing “reg=val” in hexadecimal writes the value to the register. It is used primarily to verify the registers are programmed correctly.

3 Tables

The switch has some internal tables that can only be accessed indirectly using a set of fixed registers. Those tables are Dynamic MAC Address Table, Static MAC Address Table, VLAN Table, and MIB Counters.

3.1 Register Description

Indirect Access Data Register 1 (0x027 – 0x027)

Bit	Default	R/W	Description
15-8	0x00	RO	Reserved
7	0	RO	Read in Progress
6-3	0x0	RO	Reserved
2-0	0x0	RO	Indirect Data [66:64]

Indirect Access Data Register 2 (0x028 – 0x029)

Bit	Default	R/W	Description
15-0	0x0000	RW	Indirect Data [47:32]

Indirect Access Data Register 3 (0x02A – 0x02B)

Bit	Default	R/W	Description
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15-0	0x0000	RW	Indirect Data [63:48]
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Indirect Access Data Register 4 (0x02C – 0x02D)

Bit	Default	R/W	Description
15-0	0x0000	RW	Indirect Data [15:0]

Indirect Access Data Register 5 (0x02E – 0x02F)

Bit	Default	R/W	Description
15-0	0x0000	RW	Indirect Data [31:16]

These data registers are used to pass data. When the table is in read access, the data are from the table. When the table is in write access, the data are put in registers first before programming the control register.

Indirect Access Control Register (0x030 – 0x031)

Bit	Default	R/W	Description
15-13	0x0	RW	Reserved
12	0	RW	Read Access
11-10	0x0	RW	Table Select
9-0	0x000	RW	Indirect Address [9:0]

The switch has 4 tables that require indirect access. The Table Select is used to select which table to access: 0 for static MAC table, 1 for VLAN table, 2 for dynamic MAC table, and 3 for MIB counters.

The Indirect Address specifies the index in the table.

The Read Access is set for read access, otherwise it is write access.

Port 1 MIB Counters (0x00 – 0x01F)

Port 2 MIB Counters (0x20 – 0x03F)

Port 3 MIB Counters (0x40 – 0x05F)

Bit	Default	R/W	Description
31	0	RO	Counter Overflow
30	0	RO	Counter Valid



29-0	0x00000000	RC	Counter Value
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These MIB counters are cleared after read, so software needs to keep track of them.

- Port 1 TX Dropped Packet Counters (0x100)**
- Port 2 TX Dropped Packet Counters (0x101)**
- Port 3 TX Dropped Packet Counters (0x102)**
- Port 1 RX Dropped Packet Counters (0x103)**
- Port 2 RX Dropped Packet Counters (0x104)**
- Port 3 RX Dropped Packet Counters (0x105)**

Bit	Default	R/W	Description
31-16	0	RO	Reserved
15-0	0x0000	RO	Counter Value

These MIB counters can be read as is.

Static MAC Address Table (0x0 – 0x7)

Bit	Default	R/W	Description
57-54	0b0000	RW	FID
53	0	RW	Use FID
52	0	RW	Override
51	0	RW	Valid
50-48	0b000	RW	Forwarding Ports
47-0	0	RW	MAC Address

There are 8 entries in the static MAC table.

The MAC Address specifies the MAC address for lookup.

The Forwarding Ports indicates where to forward the frames. Bit 0 is port 1, bit 2 is port 2, and bit 3 is port 3. Setting 0 means no forwarding, while setting 7 means broadcasting.

The Valid bit is used to indicate the entry is valid. Setting 0 is like deleting the entry.

The Override bit is used to override the port transmit and receive disable settings.

The Use FID bit is used to specify FID+MAC for lookup.

The FID specifies the Filter ID if FID+MAC is used.

Dynamic MAC Address Table (0x000 – 0x3FF)

Bit	Default	R/W	Description
71	0	RO	Data Not Ready
70-67	0	RO	Reserved
66	1	RO	MAC Empty
65-56	0x000	RO	Number of Valid Entries
55-54		RO	Time Stamp
53-52		RO	Source Port
51-48		RO	FID
47-0		RO	MAC Address

There can be up to 1048 entries in the dynamic MAC table.

The Data Not Ready bit means the data needs to be read again until it is ready.

The MAC Empty bit means there are no entry. With it off the actual number of entries is the Number of Valid Entries plus one. The number of entries is determined first by reading the entry at index 0. Afterward increase the index and keep reading the data until the index is past the number of entries.

The Time Stamp is a counter for internal aging.

The Source Port indicates which port the FID+MAC information is learned. Port 1 is 0, port 2 is 1, and port 3 is 2.

The FID specifies the Filter ID.

The MAC Address specifies the MAC address learned.

VLAN Table (0x0 – 0xF)

Bit	Default	R/W	Description
19	1	RW	Valid
18-16	0b111	RW	Membership
15-12	0x0	RW	FID
11-0	0x001	RW	VID

There are 16 entries in the VLAN table. Each entry associates a VLAN ID (VID) to a Filter ID (FID). The membership indicates which ports are forwarded when the lookup fails. The valid bit is used to indicate the entry is valid.

3.2 Sysfs Variables

```
sw/static_table
mac7/7_fid
mac7/7_use_fid
mac7/7_override
mac7/7_valid
mac7/7_ports
mac7/7_addr
```

The `static_table` variable displays only valid entries in the static MAC table. The format is “<entry>: <MAC address> <ports> <override> <fid>:<use fid>.”

Writing 1 to the `valid` variable will write the entry to the static MAC table. Therefore, it should be the last one to write.

```
sw/dynamic_table
```

The `dynamic_table` variable displays the entries in the dynamic MAC table. The format is “<MAC address> <port> <timestamp>.”

It can be written to flush the dynamic MAC table.

```
sw/vlan_table
vlanf/f_valid
vlanf/f_member
vlanf/f_fid
vlanf/f_vid
```

The `vlan_table` variable displays only valid entries in the VLAN table. The format is “<entry>: <VID> <FID> <membership>.”

Writing 1 to the `valid` variable will write the entry to the VLAN table. Therefore, it should be the last one to write.

```
sw/mib
sw2/2_mib
```

The `mib` variable displays the MIB counters. The counters in each port can be displayed individually.

4 Flow Control

4.1 Register Description

Switch Global Control Register 1 (0x002 – 0x003)

Bit	Default	R/W	Description
13	1	RW	IEEE 802.3x Transmit Flow Control Enable
12	1	RW	IEEE 802.3x Receive Flow Control Enable
8	0	RW	Aggressive Back-Off Enable

The default is to enable receive and transmit flow control in full-duplex mode.

It is advised to turn on Aggressive Back-Off in half-duplex mode to enhance performance.

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
5	1	RW	Back Pressure Mode
4	1	RW	Flow Control and Back Pressure Fair Mode
3	0	RW	No Excessive Collision Drop

The default Back Pressure Mode is carrier sense-based rather than collision-based.

Flow Control and Back Pressure Fair Mode is the default.

It is advised to turn on No Excessive Collision Drop in half-duplex mode.

Switch Global Control Register 3 (0x006 – 0x007)

Bit	Default	R/W	Description
6	0	RW	Switch Host Port in Half Duplex Mode
5	0	RW	Switch Host Port Flow Control Enable

The switch host port can be put in half-duplex mode. Flow control in the switch host port can be enabled in full-duplex mode.

Switch Global Control Register 8 (0x0AC – 0x0AD)

Bit	Default	R/W	Description
7-0	0x00	RW	Force PAUSE Off Iteration Limit Time

This register can be used to change the default PAUSE time. The unit number is 160 ms.

Port 1 Control Register 2 (0x06E – 0x06F)

Port 2 Control Register 2 (0x086 – 0x087)

Port 3 Control Register 2 (0x09E – 0x09F)

Bit	Default	R/W	Description
12	1	RW	Force Flow Control
11	0	RW	Back Pressure Enable

It is advised to enable back pressure when in half-duplex mode. Flow control can be forced.

Port 1 Status Register (0x080 – 0x081)

Port 2 Status Register (0x098 – 0x099)

Bit	Default	R/W	Description
12	0	RO	Receive Flow Control Active
11	0	RO	Transmit Flow Control Active

The receive and transmit flow control status can be retrieved.

4.2 Sysfs Variables

```
sw/aggr_backoff
sw/back_pressure
sw/no_exc_drop
sw/rx_flow_ctrl
sw/tx_flow_ctrl
sw/fair_flow_ctrl
sw/sw_flow_ctrl
sw/sw_half_duplex
sw/pause_time
sw1/1_rx_flow_ctrl
sw1/1_tx_flow_ctrl
sw2/2_back_pressure
sw2/2_force_flow_ctrl
```

5 MAC Address

The switch MAC address is used to send PAUSE frames. It can be programmed the same as the host MAC address.

5.1 Register Description

MAC Address Register 1 (0x010 – 0x011)

Bit	Default	R/W	Description
15-0	0x0010	RW	MAC Address [47:32]

MAC Address Register 2 (0x012 – 0x013)

Bit	Default	R/W	Description
15-0	0xA1FF	RW	MAC Address [31:16]

MAC Address Register 3 (0x014 – 0x015)

Bit	Default	R/W	Description
15-0	0xFFFF	RW	MAC Address [15:0]

5.2 Sysfs Variables

`sw/macaddr`

The format of `macaddr` is `xx:xx:xx:xx:xx:xx`.

6 Link

6.1 Register Description

PHY 1 Control Register (0x04C – 0x04D)

PHY 2 Control Register (0x058 – 0x059)

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	Far-End Loopback
13	0	RW	Force 100BT Speed
12	1	RW	Auto-Negotiation Enable
11	0	RW	Power Down
10	0	RO	Isolate
9	0	RW	Restart Auto-Negotiation
8	0	RW	Force Full Duplex
7	0	RO	Collision Test
6	0	RO	Reserved
5	1	RW	HP MDI-X Mode
4	0	RW	Force MDI-X
3	0	RW	Auto MDI/MDI-X Disable
2	0	RW	Far-End Fault Disable
1	0	RW	Transmit Disable
0	0	RW	LED Disable

PHY 1 Status Register (0x04E – 0x04F)

PHY 2 Status Register (0x05A – 0x05B)

Bit	Default	R/W	Description
15	0	RO	T4 Capable
14	1	RO	100BT Full-Duplex Capable
13	1	RO	100BT Half-Duplex Capable
12	1	RO	10BT Full-Duplex Capable
11	1	RO	10BT Half-Duplex Capable
10–7	0x0	RO	Reserved



6	0	RO	Preamble Suppressed
5	0	RO	Auto-Negotiation Done
4	0	RO	Far-End Fault
3	1	RO	Auto-Negotiation Capable
2	0	RO	Link Good
1	0	RO	Jabber Test
0	0	RO	Extended Register Capable

PHY 1 ID Low Register (0x050 – 0x051)
PHY 2 ID Low Register (0x05C – 0x05D)

Bit	Default	R/W	Description
15-0	0x1430	RO	PHY ID Low Word

PHY 1 ID High Register (0x052 – 0x053)
PHY 2 ID High Register (0x05E – 0x05F)

Bit	Default	R/W	Description
15-0	0x0022	RO	PHY ID High Word

It is noted that the order of the PHY ID registers are reversed when compared to the standard MDIO registers.

PHY 1 Auto-Negotiation Advertisement Register (0x054 – 0x055)
PHY 2 Auto-Negotiation Advertisement Register (0x060 – 0x061)

Bit	Default	R/W	Description
15	0	RO	Next Page
14	0	RO	Reserved
13	0	RO	Remote Fault
12-11	0x0	RO	Reserved
10	1	RW	Advertise Flow Control Capability
9	0	RO	Reserved
8	1	RW	Advertise 100BT Full-Duplex Capability
7	1	RW	Advertise 100BT Half-Duplex Capability
6	1	RW	Advertise 10BT Full-Duplex Capability
5	1	RW	Advertise 10BT Half-Duplex Capability



4-0	0x01	RO	Selector Field
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PHY 1 Auto-Negotiation Link Partner Capability Register (0x056 – 0x057)

PHY 2 Auto-Negotiation Link Partner Capability Register (0x062 – 0x063)

Bit	Default	R/W	Description
15	0	RO	Next Page
14-12	0x0	RO	Reserved
10	0	RO	Partner Flow Control Capable
9	0	RO	Reserved
8	0	RO	Partner 100BT Full-Duplex Capable
7	0	RO	Partner 100BT Half-Duplex Capable
6	0	RO	Partner 10BT Full-Duplex Capable
5	0	RO	Partner 10BT Half-Duplex Capable
4-0	0x01	RO	Reserved

The definitions of these registers are the same as the standard MDIO registers.

Port 1 Control Register 4 (0x07E – 0x07F)

Port 2 Control Register 4 (0x096 – 0x097)

Bit	Default	R/W	Description
15	0	RW	LED Disable
14	0	RW	Transmit Disable
13	0	RW	Restart Auto-Negotiation
12	0	RW	Far-End Fault Disable
11	0	RW	Power Down
10	0	RW	Auto MDI/MDI-X Disable
9	0	RW	Force MDI-X
8	0	RW	Far-End Loopback
7	1	RW	Auto-Negotiation Enable
6	0	RW	Force 100BT Speed
5	0	RW	Force Full Duplex
4	1	RW	Advertise Flow Control Capability
3	1	RW	Advertise 100BT Full-Duplex Capability
2	1	RW	Advertise 100BT Half-Duplex Capability



1	1	RW	Advertise 10BT Full-Duplex Capability
0	1	RW	Advertise 10BT Half-Duplex Capability

Port 1 Status Register (0x080 – 0x081)

Port 2 Status Register (0x098 – 0x099)

Bit	Default	R/W	Description
15	1	RW	HP Auto MDI-X Mode
14	0	RO	Reserved
13	0	RO	Polarity Reverse
12	0	RO	Receive Flow Control Active
11	0	RO	Transmit Flow Control Active
10	0	RO	Link Speed
9	0	RO	Link Duplex
8	0	RO	Far-End Fault
7	0	RO	MDI-X Not Active
6	0	RO	Auto-Negotiation Done
5	0	RO	Link Good
4	0	RO	Partner Flow Control Capable
3	0	RO	Partner 100BT Full-Duplex Capable
2	0	RO	Partner 100BT Half-Duplex Capable
1	0	RO	Partner 10BT Full-Duplex Capable
0	0	RO	Partner 10BT Half-Duplex Capable

These two registers map the standard PHY control and status registers into a convenient place to quickly access the PHY information. The bits with the same name as those in the standard PHY registers are mapped directly. As a result, it is recommended to use these registers to control the PHY.

6.2 Sysfs Variables

```
sw/duplex
sw/speed
sw/force
sw/flow_ctrl
sw1/1_duplex
```

sw1/1_speed

The `duplex` variable displays the duplex mode as either full-duplex or half-duplex if there is a link; otherwise it is unlinked. Writing 0 means auto, normally selecting full-duplex as the best operating mode. Writing 1 specifies half-duplex mode. Writing 2 specifies full-duplex mode.

The `speed` variable displays the speed as either 10 or 100 Mbps if there is a link; otherwise it is unlinked. Writing 0 means auto, normally selecting 100 Mbps as the best operating speed. Writing 10 specifies 10 Mbps. Writing 100 specifies 100 Mbps only.

The `force` variable specifies that auto-negotiation not to be used. Writing to it updates the registers for the new link mode.

The `flow_ctrl` variable enable flow control advertisement.

The general `duplex` and `speed` variables indicate at least one of the ports of the switch is connected. To get the status of each individual port the `port duplex` and `speed` variables can be read.

7 LinkMD

7.1 Register Description

Port 1 PHY Special Control Register 1 (0x07C– 0x07D)

Port 2 PHY Special Control Register 1 (0x094– 0x095)

Bit	Default	R/W	Description
15	0	RO	Less Than 10m
14–13	0x0	RO	LinkMD Result
12	0	SC	LinkMD Test Enable
11	0	RW	Force Link
9	0	RW	Remote Loopback
8–0	0x000	RW	LinkMD Fault Count

Port 1 Control Register 4 (0x07E – 0x07F)

Port 2 Control Register 4 (0x096 – 0x097)

Bit	Default	R/W	Description
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15	0	RW	LED Off
14	0	RW	Transmit Disable
13	0	RW	Restart Auto Negotiation
12	0	RW	Far-End Fault Disable
11	0	RW	Power Down
10	0	RW	Auto MDI/MDI-X Disable
9	0	RW	Force MDI-X
8	0	RW	Far-End Loopback
7	0	RW	Auto Negotiation Enable
6	0	RW	Force Speed
5	0	RW	Force Duplex
4	0	RW	Advertise Flow Control Capability
3	0	RW	Advertise 100BT Full-Duplex Capability
2	0	RW	Advertise 100BT Half-Duplex Capability
1	0	RW	Advertise 10BT Full-Duplex Capability
0	0	RW	Advertise 10BT Half-Duplex Capability

Port 1 Status Register (0x080 – 0x081)

Port 2 Status Register (0x098 – 0x099)

Bit	Default	R/W	Description
15	1	RW	HP Auto MDI-X Mode
14	0	RO	Reserved
13	0	RO	Polarity Reverse
12	0	RO	Receive Flow Control Active
11	0	RO	Transmit Flow Control Active
10	0	RO	Link Speed
9	0	RO	Link Duplex
8	0	RO	Far-End Fault
7	0	RO	MDI-X Not Active
6	0	RO	Auto-Negotiation Done
5	0	RO	Link Good
4	0	RO	Partner Flow Control Capable
3	0	RO	Partner 100BT Full-Duplex Capable
2	0	RO	Partner 100BT Half-Duplex Capable



1	0	RO	Partner 10BT Full-Duplex Capable
0	0	RO	Partner 10BT Half-Duplex Capable

7.2 Sysfs Variables

`swl/1_linkmd`

Writing to the linkmd variable starts the LinkMD test. Reading from the variable displays a string in the format “[overall length:overall status] [pair 1 length: pair 1 status] [pair 2 length:pair 2 status].” The meaning of the status is 0 for unknown, 1 for good,

8 Huge Frame

The switch supports transmitting and receiving frames with length longer than the standard 1518 bytes. The maximum length supported is 1916 bytes.

8.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
2	0	RW	Huge Packet Support
1	0	RW	Legal Maximum Packet Size Check Enable

The Huge Packet Support allows packet size up to 1916 bytes.

The Legal Maximum Packet Size Check allows packet size of 1522 bytes for tagged packets and 1518 bytes for untagged packets. Otherwise, the maximum packet size is 1536 bytes.

8.2 Sysfs Variables

`sw/huge_packet`
`sw/legal_packet`

9 Aging

Aging allows the switch lookup engine to discard records that are not updated for a certain time. This frees up space in the dynamic MAC table and minimizes lookup time. The normal aging period is about 200 seconds.

9.1 Register Description

Switch Global Control Register 1 (0x002 – 0x003)

Bit	Default	R/W	Description
19	1	RW	Aging Enable
9	0	RW	Fast Aging Enable
0	0	RW	Link Change Aging Enable

Aging is enabled by default. Fast Aging reduces the aging period to microseconds. It is used normally in support to Spanning Tree Protocol. Link Change Aging allows the switch to flush the MAC table when the cable is disconnected. It is normally good practice to enable it. However, the feature is not working in this hardware revision.

Switch Global Control Register 8 (0x0AC – 0x0AD)

Bit	Default	R/W	Description
10	0	RW	Flush Dynamic MAC Table

The dynamic MAC address table can be flushed on command. However, it requires the port learning to be disabled first. Basically this command removes all entries of the port that stops learning.

9.2 Sysfs Variables

```
sw/aging
sw/fast_aging
sw/link_aging
```

10 Broadcast Storm Protection

Broadcast Storm Protection protects the switch system from receiving too many broadcast packets. A rate can be set to specify how much broadcast packets are allowed to forward. There is an option to include multicast packets in this protection.

10.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
6	1	RW	Multicast Storm Protection Disable

Multicast Storm Protection is normally disabled.

Switch Global Control Register 3 (0x006 – 0x007)

Bit	Default	R/W	Description
15-8	0x63	RW	Broadcast Storm Protection Rate [7:0]
2-0	0x0	RW	Broadcast Storm Protection Rate [10:8]

The default storm protection rate is 1%. The rate value is calculated as $(148800 * 67 * 1 / 100 / 1000 = 0x63)$. It is broken in two parts when programmed to the register.

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
7	0	RW	Broadcast Storm Protection Enable

The Broadcast Storm Protection can be enabled in each port individually.

10.2 Sysfs Variables

```
sw/mcast_storm  
sw/bcast_per
```

sw2/2_bcast_storm

The `bcast_per` variable displays the storm protection rate in percentage. The maximum value is about 21%.

11 Port Source Address Filtering

The switch can filter out packets sent by its own ports in a ring topology. For that to work a MAC address has to be assigned to each port. Normally it will be the same as the host MAC address.

11.1 Register Description

Port 1 Source Address Filtering MAC Address Register 1 (0x0B0 – 0x0B1)
Port 2 Source Address Filtering MAC Address Register 1 (0x0B6 – 0x0B7)

Bit	Default	R/W	Description
15-0	0x0000	RW	MAC Address [15:0]

Port 1 Source Address Filtering MAC Address Register 2 (0x0B2 – 0x0B3)
Port 2 Source Address Filtering MAC Address Register 2 (0x0B8 – 0x0B9)

Bit	Default	R/W	Description
15-0	0x0000	RW	MAC Address [31:16]

Port 1 Source Address Filtering MAC Address Register 3 (0x0B4 – 0x0B5)
Port 2 Source Address Filtering MAC Address Register 3 (0x0BA – 0x0BB)

Bit	Default	R/W	Description
15-0	0x0000	RW	MAC Address [47:32]

The port source address normally is the same as the host MAC address. Addresses in both ports normally are the same unless the host separates the ports and has two network devices.

Port 1 Control Register 1 (0x06C – 0x06D)
Port 2 Control Register 1 (0x084 – 0x085)

Bit	Default	R/W	Description
11	0	RW	Source Address Filtering Enable for Port 2
10	0	RW	Source Address Filtering Enable for Port 1

The Source Address Filtering can be enabled in each port to filter address from either port 1 or 2 or both.

11.2 Sysfs Variables

```
sw1/1_macaddr
sw1/1_src_filter_0
sw1/1_src_filter_1
```

The format of `macaddr` is `xx:xx:xx:xx:xx:xx`.

12 Spanning Tree Support

12.1 Register Description

Port 1 Control Register 2 (0x06E – 0x06F)

Port 2 Control Register 2 (0x086 – 0x087)

Port 3 Control Register 2 (0x09E – 0x09F)

Bit	Default	R/W	Description
10	1	RW	Transmit Enable
9	1	RW	Receive Enable
8	0	RW	Learning Disable

The port can be shut off by disabling transmit and receive. The learning can be turned off depending on STP state.

Switch Global Control Register 8 (0x0AC – 0x0AD)

Bit	Default	R/W	Description
10	0	SC	Flush Dynamic MAC Table

9	0	SC	Flush Static MAC Table
---	---	----	-------------------------------

The learning of the 3 ports need to be disabled first before the whole dynamic MAC table can be flushed with the Flush Dynamic MAC Table command. The Flush Static MAC Table command does not work.

12.2 Sysfs Variables

```
sw2/2_rx
sw2/2_tx
sw2/2_learn
```

13 Tail Tagging

Tail Tagging is a feature in which the switch attaches a tag at the end of packet to indicate the source port when forwarded to the host port. The host then has a way to determine the source of the packet. The host can attach the tag when transmitting to specify the destination ports.

13.1 Register Description

Switch Global Control Register 8 (0x0AC – 0x0AD)

Bit	Default	R/W	Description
8	0	RW	Tail Tag Enable

After tail tagging is enabled the host needs to make sure the tag at the end of transmit packet is set correctly to ensure proper operation.

The incoming tag shows either 0 for port 1 or 1 for port 2. The outgoing tag can be 0 for normal lookup, 1 for port 1, 2 for port 2, and 3 for broadcasting. The bits 2 and 3 can store the frame priority 0 to 3.

13.2 Sysfs Variables

```
sw/tail_tag
```

14 IGMP Snooping

IGMP Snooping allows Internet Group Management Protocol (IGMP) packets to be forwarded to the host port so that software can setup the Static MAC Address Table to limit the broadcasting of multicast packets. Tail Tagging mode need to be enabled so that software knows which port the IGMP packet is received.

14.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
14	0	RW	IGMP Snooping Enable

14.2 Sysfs Variables

```
sw/igmp_snoop
```

15 IPv6 MLD Snooping

IPv6 MLD Snooping is similar to IGMP Snooping but works for IPv6 packets. It allows Multicast Listener Discovery (MLD) packets to be forwarded to the host port so that software can setup the Static MAC Address Table to limit the broadcasting of multicast packets.

15.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
13	0	RW	IPv6 MLD Snooping Enable
12	0	RW	IPv6 MLD Snooping Option

IPv6 MLD Snooping allows IPv6 packets with next header equals to 1 or 58 to be forwarded to the host port.

IPv6 MLD Snooping Option allows IPv6 packets with next header equals to 43, 44, 50, 51, or 60 to be forwarded to the host port.

15.2 Sysfs Variables

```
sw/ipv6_mld_snoop  
sw/ipv6_mld_option
```

16 Port Mirroring

Port Mirroring allows network traffic among ports to be routed to a specific port for network monitoring and debugging purpose.

16.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
8	0	RW	Sniff Mode Select

The default sniff mode is RX or TX, meaning either the source port or destination port needs to match. This is the mode used to implement RX only sniff. Setting 1 selects RX and TX sniff mode, meaning both the source port and destination need to match. This can narrow down the mirrored traffic to a specific path.

Port 1 Control Register 2 (0x06E – 0x06F)

Port 2 Control Register 2 (0x086 – 0x087)

Port 3 Control Register 2 (0x09E – 0x09F)

Bit	Default	R/W	Description
7	0	RW	Sniffer Port
6	0	RW	Receive Sniff
5	0	RW	Transmit Sniff

Each port can turn on receive or transmit mirroring. At least one needs to be a sniffer port.

16.2 Sysfs Variables

```
sw/mirror_mode  
sw2/2_mirror_rx  
sw2/2_mirror_tx  
sw2/2_mirror_port
```

17 VLAN

17.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
15	0	RW	802.1Q VLAN Enable
7	1	RW	Unicast Port-VLAN Mismatch Discard

VLAN table needs to be setup first before turning on VLAN. Unicast Port-VLAN Mismatch Discard makes sure no packets can cross the VLAN boundary.

Switch Global Control Register 3 (0x006 – 0x007)

Bit	Default	R/W	Description
3	0	RW	Null VID Replacement

Null VID Replacement replaces the NULL VID with the port VID value.

Switch Global Control Register 9 (0x0AE – 0x0AF)

Bit	Default	R/W	Description
10-8	0x0	RW	Forward Invalid VID Frame to Ports

Frames with invalid VID can be forwarded to each port.

Port 1 Control Register 2 (0x06E – 0x06F)

Port 2 Control Register 2 (0x086 – 0x087)

Port 3 Control Register 2 (0x09E – 0x09F)

Bit	Default	R/W	Description
14	0	RW	Ingress VLAN Filtering
13	0	RW	Discard Non PVID Packets
3	0	RW	User Priority Ceiling
2-0	0x7	RW	Port VLAN Membership

Ingress VLAN filtering discards VLAN packets that do not match the port VID.

Discard Non PVID Packets discards VLAN packets with zero VID.

User Priority Ceiling can remap 802.1p priority in the VLAN packets with the one defined in the port.

Port VLAN Membership defines the membership of the port.

Port 1 VID Control Register (0x070 – 0x071)

Port 2 VID Control Register (0x088 – 0x089)

Port 3 VID Control Register (0x0A0 – 0x0A1)

Bit	Default	R/W	Description
15-13	0	RW	User Priority Field of VLAN Tag
12	0	RW	CFI of VLAN Tag
11-0	0x001	RW	VID of VLAN Tag

The VID defined for each port is used in several switch functions.

The User Priority Field can be used for 802.1p priority remapping.

17.2 Sysfs Variables

```
sw/vlan
sw/null_vid
sw/vlan_bound
sw2/2_member
sw2/2_vid
```

```
sw2/2_fw_inv_vid
sw2/2_ingress
sw2/2_non_vid
sw2/2_replace_prio
```

17.3 Tag Insertion

VLAN tag insertion allows two VLANs with tagged and untagged packets coexist.

17.3.1 Register Description

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
2	0	RW	Tag Insertion

VLAN tag can be inserted with the VID defined in each port individually.

Switch Global Control Register 9 (0x0AE – 0x0AF)

Bit	Default	R/W	Description
5	0	RW	Insert Source Port PVID Tag From Port 3 to Port 2
4	0	RW	Insert Source Port PVID Tag From Port 3 to Port 1
3	0	RW	Insert Source Port PVID Tag From Port 2 to Port 3
2	0	RW	Insert Source Port PVID Tag From Port 2 to Port 1
1	0	RW	Insert Source Port PVID Tag From Port 1 to Port 3
0	0	RW	Insert Source Port PVID Tag From Port 1 to Port 2

17.3.2 Sysfs Variables

```
sw/ins_0_to_1
sw/ins_0_to_2
```

```
sw/ins_1_to_0  
sw/ins_1_to_2  
sw/ins_2_to_0  
sw/ins_2_to_1  
sw2/2_ins_tag
```

17.4 Tag Removal

VLAN tag removal allows two VLANs with tagged and untagged packets coexist.

17.4.1 Register Description

Port 1 Control Register 1 (0x06C – 0x06D)
Port 2 Control Register 1 (0x084 – 0x085)
Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
1	0	RW	Tag Removal

VLAN tag can be removed in each port individually.

17.4.2 Sysfs Variables

```
sw2/2_rmv_tag
```

17.5 Drop Tagged Packet

17.5.1 Register Description

Port 1 Control Register 1 (0x06C – 0x06D)
Port 2 Control Register 1 (0x084 – 0x085)
Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
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9	0	RW	Drop Tagged Packet
---	---	----	--------------------

17.5.2 Sysfs Variables

sw2/2_drop_tagged

18 QoS

18.1 Priority Queues

18.1.1 Register Description

Switch Global Control Register 2 (0x004 – 0x005)

Bit	Default	R/W	Description
0	0	RW	Priority Buffer Reserve

Each port is pre-allocated 48 buffers used exclusively for high priority (q3, q2, and q1) packets when multiple queue feature is turned on.

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
8	0	RW	TX Two Queues Select Enable
0	0	RW	TX Multiple Queues Select Enable

Multiple priority queues can be turned on in each port. They are needed for QoS priority.

Port 1 TX Queue Rate Control Register 1 (0x0C8– 0x0C9)

Port 2 TX Queue Rate Control Register 1 (0x0CC– 0x0CD)

Port 3 TX Queue Rate Control Register 1 (0x0D0– 0x0D1)

Bit	Default	R/W	Description
15	1	RW	TX Queue 2 Ratio Control
14-8	0x04	RW	TX Queue 2 Ratio
7	1	RW	TX Queue 3 Ratio Control
6-0	0x08	RW	TX Queue 3 Ratio

Port 1 TX Queue Rate Control Register 2 (0x0CA– 0x0CB)

Port 2 TX Queue Rate Control Register 2 (0x0CE– 0x0CF)

Port 3 TX Queue Rate Control Register 2 (0x0D2– 0x0D3)

Bit	Default	R/W	Description
15	1	RW	TX Queue 0 Ratio Control
14-8	0x01	RW	TX Queue 0 Ratio
7	1	RW	TX Queue 1 Ratio Control
6-0	0x02	RW	TX Queue 1 Ratio

The transmit priority in each queue can be controlled individually. Setting 0 to Queue Ratio Control means all packets in this priority queue are transmitted before transmitting packets in lower priority queues. The Queue Ratio indicates the number of packets allowed to transmit within a certain time. Normally higher priority queues can transmit more packets than lower priority queues. If those numbers are changed in an illogical way, the queue priority can be switched.

18.1.2 Sysfs Variables

```
sw/buf_reserve
sw2/2_prio_queue
sw2/2_tx_p0_ctrl
sw2/2_tx_p0_ratio
sw2/2_tx_p1_ctrl
sw2/2_tx_p1_ratio
sw2/2_tx_p2_ctrl
sw2/2_tx_p2_ratio
sw2/2_tx_p3_ctrl
sw2/2_tx_p3_ratio
```

18.2 Port-Based Priority

18.2.1 Register Description

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
4–3	0x0	RW	Port-Based Priority Select

If DiffServ or 802.1p priority is not enabled then port-based priority is used. The queue priorities are 0, 1, 2, and 3.

18.2.2 Sysfs Variables

`sw2/2_port_based`

18.3 802.1p Priority

18.3.1 Register Description

Switch Global Control Register 6 (0x00C – 0x00D)

Bit	Default	R/W	Description
15–14	0x3	RW	IEEE 802.1p mapping of frame's priority with tag 7
13–12	0x3	RW	IEEE 802.1p mapping of frame's priority with tag 6
11–10	0x2	RW	IEEE 802.1p mapping of frame's priority with tag 5
9–8	0x2	RW	IEEE 802.1p mapping of frame's priority with tag 4
7–6	0x1	RW	IEEE 802.1p mapping of frame's priority with tag 3
5–4	0x1	RW	IEEE 802.1p mapping of frame's priority with tag 2
3–2	0x0	RW	IEEE 802.1p mapping of frame's priority with tag 1
1–0	0x0	RW	IEEE 802.1p mapping of frame's priority with tag 0

The 802.1p priority has 8 tags, 0 to 7. Each tag can be mapped to a queue priority from 0 to 3.

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
5	0	RW	802.1p Priority Enable

The 802.1p priority can be turned on in each port individually.

18.3.2 Sysfs Variables

```
sw/p_802_1p_map
sw2/2_p_802_1p
```

The `p_802_1p_map` variable displays the priority queue mapping of the 8 tags. To change the mapping the users need to pass the information in the format of “<tag>=<queue>.” The tag value should be less than 8, and the queue value should be less than 4. To enter the information quickly the value can be more than 3 to indicate the value is for more than 1 tag. For a value 3 or less it is meant for 1 tag; 0xf or less, 2 tags; 0xff or less, 4 tags; and 0xffff or less, 8 tags.

18.4 DiffServ Priority

18.4.1 Register Description

TOS Priority Control Register 1 (0x016 – 0x017)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0x1c [15:14]
13-12	0	RW	DiffServ mapping of frame's priority with value 0x18 [13:12]
11-10	0	RW	DiffServ mapping of frame's priority with value 0x14 [11:10]
9-8	0	RW	DiffServ mapping of frame's priority with value 0x10 [9:8]
7-6	0	RW	DiffServ mapping of frame's priority with value 0x0c [7:6]
5-4	0	RW	DiffServ mapping of frame's priority with value 0x08 [5:4]
3-2	0	RW	DiffServ mapping of frame's priority with value 0x04 [3:2]
1-0	0	RW	DiffServ mapping of frame's priority with value 0x00 [1:0]

TOS Priority Control Register 2 (0x018 – 0x019)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0x3c [31:30]
13-12	0	RW	DiffServ mapping of frame's priority with value 0x38 [29:28]
11-10	0	RW	DiffServ mapping of frame's priority with value 0x34 [27:26]
9-8	0	RW	DiffServ mapping of frame's priority with value 0x30 [25:24]
7-6	0	RW	DiffServ mapping of frame's priority with value 0x2c [23:22]
5-4	0	RW	DiffServ mapping of frame's priority with value 0x28 [21:20]
3-2	0	RW	DiffServ mapping of frame's priority with value 0x24 [19:18]
1-0	0	RW	DiffServ mapping of frame's priority with value 0x20 [17:16]

TOS Priority Control Register 3 (0x01A – 0x01B)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0x5c [47:46]
13-12	0	RW	DiffServ mapping of frame's priority with value 0x58 [45:44]
11-10	0	RW	DiffServ mapping of frame's priority with value 0x54 [43:42]
9-8	0	RW	DiffServ mapping of frame's priority with value 0x50 [41:40]
7-6	0	RW	DiffServ mapping of frame's priority with value 0x4c [39:38]
5-4	0	RW	DiffServ mapping of frame's priority with value 0x48 [37:36]
3-2	0	RW	DiffServ mapping of frame's priority with value 0x44 [35:34]
1-0	0	RW	DiffServ mapping of frame's priority with value 0x40 [33:32]

TOS Priority Control Register 4 (0x01C – 0x01D)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0x7c [63:62]
13-12	0	RW	DiffServ mapping of frame's priority with value 0x78 [61:60]
11-10	0	RW	DiffServ mapping of frame's priority with value 0x74 [59:58]
9-8	0	RW	DiffServ mapping of frame's priority with value 0x70 [57:56]
7-6	0	RW	DiffServ mapping of frame's priority with value 0x6c [55:54]
5-4	0	RW	DiffServ mapping of frame's priority with value 0x68 [53:52]
3-2	0	RW	DiffServ mapping of frame's priority with value 0x64 [51:50]



1-0	0	RW	DiffServ mapping of frame's priority with value 0x60 [49:48]
-----	---	----	--

TOS Priority Control Register 5 (0x01E – 0x01F)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0x9c [79:78]
13-12	0	RW	DiffServ mapping of frame's priority with value 0x98 [77:76]
11-10	0	RW	DiffServ mapping of frame's priority with value 0x94 [75:74]
9-8	0	RW	DiffServ mapping of frame's priority with value 0x90 [73:72]
7-6	0	RW	DiffServ mapping of frame's priority with value 0x8c [71:70]
5-4	0	RW	DiffServ mapping of frame's priority with value 0x88 [69:68]
3-2	0	RW	DiffServ mapping of frame's priority with value 0x84 [67:66]
1-0	0	RW	DiffServ mapping of frame's priority with value 0x80 [65:64]

TOS Priority Control Register 6 (0x020 – 0x021)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0xbc [95:94]
13-12	0	RW	DiffServ mapping of frame's priority with value 0xb8 [93:92]
11-10	0	RW	DiffServ mapping of frame's priority with value 0xb4 [91:90]
9-8	0	RW	DiffServ mapping of frame's priority with value 0xb0 [89:88]
7-6	0	RW	DiffServ mapping of frame's priority with value 0xac [87:86]
5-4	0	RW	DiffServ mapping of frame's priority with value 0xa8 [85:84]
3-2	0	RW	DiffServ mapping of frame's priority with value 0xa4 [83:82]
1-0	0	RW	DiffServ mapping of frame's priority with value 0xa0 [81:80]

TOS Priority Control Register 7 (0x022 – 0x023)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0xdc [111:110]
13-12	0	RW	DiffServ mapping of frame's priority with value 0xd8 [109:108]
11-10	0	RW	DiffServ mapping of frame's priority with value 0xd4 [107:106]
9-8	0	RW	DiffServ mapping of frame's priority with value 0xd0 [105:104]
7-6	0	RW	DiffServ mapping of frame's priority with value 0xcc [103:102]
5-4	0	RW	DiffServ mapping of frame's priority with value 0xc8 [101:100]

3-2	0	RW	DiffServ mapping of frame's priority with value 0xc4 [99:98]
1-0	0	RW	DiffServ mapping of frame's priority with value 0xc0 [97:96]

TOS Priority Control Register 8 (0x024 – 0x025)

Bit	Default	R/W	Description
15-14	0	RW	DiffServ mapping of frame's priority with value 0xfc [127:126]
13-12	0	RW	DiffServ mapping of frame's priority with value 0xf8 [125:124]
11-10	0	RW	DiffServ mapping of frame's priority with value 0xf4 [123:122]
9-8	0	RW	DiffServ mapping of frame's priority with value 0xf0 [121:120]
7-6	0	RW	DiffServ mapping of frame's priority with value 0xec [119:118]
5-4	0	RW	DiffServ mapping of frame's priority with value 0xe8 [117:116]
3-2	0	RW	DiffServ mapping of frame's priority with value 0xe4 [115:114]
1-0	0	RW	DiffServ mapping of frame's priority with value 0xe0 [113:112]

The DiffServ priority has 64 TOS/DiffServ/Class values. Each value can be mapped to a queue priority from 0 to 3.

Port 1 Control Register 1 (0x06C – 0x06D)

Port 2 Control Register 1 (0x084 – 0x085)

Port 3 Control Register 1 (0x09C – 0x09D)

Bit	Default	R/W	Description
6	0	RW	DiffServ Priority Enable

The DiffServ priority can be turned on in each port individually.

18.4.2 Sysfs Variables

```
sw/diffserv_map  
sw2/2_diffserv
```

The `diffserv_map` variable displays the priority queue mapping of the 64 DiffServ classes. To change the mapping the users need to pass the information in the format of “<class>=<queue>.” The class value should be less than 64, and the queue value should be less than 4. To enter the information quickly the value can be more than 3 to indicate the value is for more than 1 class. For a value 3 or less it is meant for 1 class; 0xf or less, 2 classes; 0xff or less, 4 classes; and 0xffff or less, 8 classes.

18.5 Rate Limiting

18.5.1 Register Description

Port 1 Control Register 3 (0x072 – 0x073)

Port 2 Control Register 3 (0x08A – 0x08B)

Port 3 Control Register 3 (0x0A2 – 0x0A3)

Bit	Default	R/W	Description
3–2	0x0	RW	Ingress Limit Mode
1	0	RW	Count Inter Frame Gap
0	0	RW	Count Preamble

The Ingress Limit Mode selects what frames are counted and limited. Mode 0 means all frames; mode 1 means broadcast, multicast, and flooded unicast frames; mode 2 means broadcast and multicast frames; and mode 3 means broadcast frames only.

Count Inter Frame Gap also counts IFG bytes, which are 12 per frame.

Count Preamble also counts preamble bytes, which are 8 per frame.

Port 1 Ingress Rate Control Register 1 (0x074 – 0x075)

Port 2 Ingress Rate Control Register 1 (0x08C – 0x08D)

Port 3 Ingress Rate Control Register 1 (0x0A4 – 0x0A5)

Bit	Default	R/W	Description
15	0	RO	Reserved
14–8	0x00	RW	Ingress Data Rate Limit for Priority 1 Frames
7	0	RO	Reserved
6–0	0x00	RW	Ingress Data Rate Limit for Priority 0 Frames

Port 1 Ingress Rate Control Register 2 (0x076 – 0x077)

Port 2 Ingress Rate Control Register 2 (0x08E – 0x08F)

Port 3 Ingress Rate Control Register 2 (0x0A6 – 0x0A7)

Bit	Default	R/W	Description
15	0	RO	Reserved



14-8	0x00	RW	Ingress Data Rate Limit for Priority 3 Frames
7	0	RO	Reserved
6-0	0x00	RW	Ingress Data Rate Limit for Priority 2 Frames

Port 1 Egress Rate Control Register 1 (0x078– 0x079)
Port 2 Egress Rate Control Register 1 (0x090– 0x091)
Port 3 Egress Rate Control Register 1 (0x0A8– 0x0A9)

Bit	Default	R/W	Description
15	0	RO	Reserved
14-8	0x00	RW	Egress Data Rate Limit for Priority 1 Frames
7	0	RO	Reserved
6-0	0x00	RW	Egress Data Rate Limit for Priority 0 Frames

Port 1 Egress Rate Control Register 2 (0x07A – 0x07B)
Port 2 Egress Rate Control Register 2 (0x092 – 0x093)
Port 3 Egress Rate Control Register 2 (0x0AA – 0x0AB)

Bit	Default	R/W	Description
15	0	RO	Reserved
14-8	0x00	RW	Egress Data Rate Limit for Priority 3 Frames
7	0	RO	Reserved
6-0	0x00	RW	Egress Data Rate Limit for Priority 2 Frames

The ingress and egress rate limits can be controlled in each port individually.

The data rate limit value is calculated using the following table. A value of zero means full rate with no limit. A value of 1 to 100 means from 1 Mbps to 100 Mbps. After that a value of 0x65 means 64 Kbps. Each value increment means 64 Kbps increase.

Data Rate	Value
1 Mbps	0x01
10 Mbps	0x0A
100 Mbps	0x64
64 Kbps	0x65
128 Kbps	0x66
192 Kbps	0x67

256 Kbps	0x68
320 Kbps	0x69
384 Kbps	0x6A
448 Kbps	0x6B
512 Kbps	0x6C
576 Kbps	0x6D
640 Kbps	0x6E
704 Kbps	0x6F
768 Kbps	0x70
832 Kbps	0x71
896 Kbps	0x72
960 Kbps	0x73

18.5.2 Sysfs Variables

```
sw2/2_prio_rate  
sw2/2_rx_limit  
sw2/2_cnt_ifg  
sw2/2_cnt_pre  
sw2/2_rx_p0_rate  
sw2/2_rx_p1_rate  
sw2/2_rx_p2_rate  
sw2/2_rx_p3_rate  
sw2/2_tx_p0_rate  
sw2/2_tx_p1_rate  
sw2/2_tx_p2_rate  
sw2/2_tx_p3_rate
```

The `prio_rate` variable is used to enable or disable rate limit function of the switch. Writing 0 means programming ingress and egress rate control registers to zero. Writing 1 means programming whatever values stored in the priority queue rate control variables.

As a result, writing to a priority queue rate control variable with a value other than zero means enabling rate limit.

The legitimate values for queue rate control variables are 0, values in multiple of 64 through 960, and values in multiple of 1000 through 100000.

19 MAC Address Filtering

When a unicast MAC address is not learned in the switch, it is termed as an unknown destination address and the packet is broadcasted to all other ports. To disable this broadcasting the switch can be setup to only forward those unknown destination packets to certain ports.

19.1 Register Description

Switch Global Control Register 7 (0x00E – 0x00F)

Bit	Default	R/W	Description
15-10	0x00	RW	Reserved
9-8	0x0	RW	Port LED Mode Select
7	0	RW	Unknown Default Port Enable
2-0	0x7	RW	Unknown Destination Packet Default Ports

The high byte of this register has a hardware error in which the bits need to be shifted left by 3 when programming the register. That means a value 0xffxx written to the register will return 0x1fxx. It is advised to access this register in 8-bit when manipulating the Unknown Destination Address feature.

19.2 Sysfs Variables

```
sw/fw_unk_dest  
sw2/2_fw_unk_dest
```

The general `fw_unk_dest` variable is used to enable the forward unknown address destination packet feature. Each port can be turned off to not forward those packets.

20 Debugging

20.1 Register Description

Switch Global Control Register 1 (0x002 – 0x003)



Bit	Default	R/W	Description
15	0	RW	Pass All Frames
3	0	RW	Pass Flow Control Packets

The Pass All Frames bit is used together with Port Mirroring for debug purpose only.

The Pass Flow Control Packets bit can be used to debug flow control.

20.2 Sysfs Variables

```
sw/pass_all  
sw/pass_pause
```