16-bit CPU Self-Test Library User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before you use the 16-bit CPU Self-test Library. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- Recommended Reading
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the 16-bit CPU Self-test Library as a development and demonstration tool for dsPIC33F, dsPIC33E, PIC24H, and PIC24E device capabilities and features. The document layout is as follows:

- **Chapter 1. Introduction –** This chapter introduces the 16-bit CPU Self-test Library and provides an overview of its features.
- **Chapter 2. Algorithm Flow** – This chapter describes the general execution flow of the 16-bit CPU Self-test Library algorithm.
- **Chapter 3. "Test Software Subsets"** – This appendix provides an overview and the computational resource requirements of the test subsets that are provided with the 16-bit CPU Self-test Library.
- **Chapter 4. Functional Test Coverage** – This chapter describes the instruction classes that are supported by the 16-bit CPU Self-test Library.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending in the Warranty Registration Card entitles you to receive new product updates. Interim software releases are available at the Microchip web site.

RECOMMENDED READING

This user's guide describes how to use the 16-bit CPU Self-test Library. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources. The latest documentation is available from the Microchip web site (www.microchip.com).

Readme Files

For the latest information on using other tools, read the tool-specific Readme files in the Readme subdirectory of the MPLAB® IDE installation directory. The Readme files contain update information and known issues that may not be included in this user's guide.

Family Reference Manual Sections

Family Reference Manual sections are available, which explain the operation of the dsPIC33F/PIC24H and dsPIC33E/PIC24H device architecture and peripheral modules. The specifics of each device family are discussed in the individual family's device data sheet.

Device Data Sheets and Flash Programming Specifications

Refer to the appropriate device data sheet for device-specific information and specifications. Also, refer to the appropriate device Flash Programming Specification for information on instruction sets and firmware development. These documents may be obtained from the Microchip web site or your local sales office.

16-bit MCU and DSC Programmer's Reference Manual (DS70157)

This manual is a software developer's reference for the 16-bit PIC24E, PIC24F, and PIC24H MCU, and 16-bit dsPIC30F, dsPIC33E, and dsPIC33F DSC families of devices. It describes the instruction set in detail and also provides general information to assist in developing software for these device families.

MPLAB® Assembler Linker and Utilities for PIC24 MCUs and dsPIC® DSCs User's Guide (DS51317)

This document details Microchip Technology's language tools for dsPIC® DSC devices based on GNU technology. The language tools discussed are:

- MPLAB Assembler PIC24 MCUs and dsPIC® DSCs
- MPLAB Linker PIC24 MCUs and dsPIC® DSCs
- MPLAB Archiver/Librarian PIC24 MCUs and dsPIC® DSCs
- Other utilities

MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide (DS51284)

This document details the use of Microchip's MPLAB C Compiler for PIC24 MCUs and dsPIC DSC devices to develop an application. The MPLAB C Compiler is a GNU-based language tool, based on source code from the Free Software Foundation (FSF). For more information about the FSF, see www.fsf.org.

MPLAB® REAL ICE™ In-Circuit Emulator User's Guide (DS51616)

This document describes how to use the MPLAB REAL ICE in-circuit emulator as a development tool to emulate and debug firmware on a target board, as well as how to program devices.

MPLAB® IDE User's Guide (DS51519)

This document describes how to use the MPLAB IDE Integrated Development Environment, as well as the MPLAB project manager, MPLAB editor and MPLAB SIM simulator. Use these development tools to help you develop and debug application code.

THE MICROCHIP WEB SITE

Microchip provides online support through our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

DEVELOPMENT SYSTEMS CUSTOMER CHANGE NOTIFICATION SERVICE

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The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers and other language tools. These include the MPLAB® C compiler; MPASM™ and MPLAB 16-bit assemblers; MPLINK™ and MPLAB 16-bit object linkers; and MPLIB™ and MPLAB 16-bit object librarians.
- **Emulators** – The latest information on the Microchip MPLAB REAL ICE™ in-circuit emulator.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 3.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 device programmer and the PICkit™ 3 development programmers.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or FAE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through our web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (June 2012)

This is the initial released version of the document.

Chapter 1. Introduction

The 16-bit CPU Self-test Library is intended to periodically verify during run-time, that all CPU core features are functioning correctly. This library supports the dsPIC33F, PIC24H, dsPIC33E and PIC24E device families.

The 16-bit CPU Self-test Library functions will simply generate some computed results that can either be logged or transmitted through any communication interface to a secondary processor in the system. The interpretation of these results that are used to determine whether the CPU is functioning correctly (and to shut down the system if a failure is detected), is the responsibility of this secondary processor. The 16-bit CPU Self-test Library test suite is not meant to test peripheral functionality, but simply that of the CPU core.

1.1 KEY REQUIREMENTS

The 16-bit CPU Self-test Library functions are executed by the CPU during application program execution and has been designed to satisfy the following general requirements:

- The 16-bit CPU Self-test Library has been implemented using the MPLAB® ASM30 assembly language programs; however, each function in the library is Callable.
- Each execution of the self-test algorithm must perform a series of computations on an original "seed" value, generating a unique 16-bit result at the end of the execution. Intermediate results based on the seed must not be overwritten by a constant value, as this would end up eliminating part of the self-test coverage.
- Each result may either be logged by the application or transmitted to a secondary processor using an available communication interface such as SPI.
- The functions in the 16-bit CPU Self-test Library may be called by the application program or real-time operating system at regular intervals. For example, the application can call each function of the 16-bit CPU Self-test Library every 2 microseconds.
- The self-test algorithm is designed to provide at least 95% test coverage of CPU functionality, which includes all available instruction opcodes, addressing modes, bus structures, bits of CPU registers, math hardware, and any special features unique to the supplier's processor that can impact the data computation. The functional test coverage is explained in detail in **Chapter 4. "Functional Test Coverage"**.

In addition, the algorithm has been designed to satisfy the following timing and computational resource constraints:

- The minimum (worst-case) CPU clock frequency that is assumed for calculating the algorithm execution time requirements is 20 MIPS.

Note: This minimum frequency is used solely for determining the library's real-time execution characteristics, and does not in any way limit the application's execution requirements (e.g., an application might need to run at lower speeds at certain times in order to minimize power consumption).

- Each individual function call in the 16-bit CPU Self-test Library must not inhibit or delay the scheduled execution of the primary control loop of the application by more than 10 microseconds. This limit represents the maximum time for which interrupts can be disabled in the application. For a minimum CPU clock frequency of 20 MIPS, this translates to 200 instruction cycles per function.
- A minimum of eight independent test results are computed every 16 ms. For a minimum CPU clock frequency of 20 MIPS, the entire test-suite is completed within 16 ms and each individual test result is generated at 2 ms intervals, which meets and exceeds the requirement. This is accomplished by partitioning the self-test algorithm into eight "test subsets", as described in **Chapter 3. "Test Software Subsets"**.
- No more than 2.5% of the overall CPU bandwidth may be utilized by the self-test routines over any 16 ms time window. For a 20 MIPS CPU clock frequency, this translates to 8000 instruction cycles (20000000 * 0.025 * 0.01)for the entire CPU test-suite. In the 16-bit CPU Self-test Library, eight test subsets are executed during each 16 ms window, and each test subset is designed to execute within only 100 instruction cycles. This implies that the execution of the entire test suite requires only 800 instruction cycles, which meets and greatly exceeds the maximum CPU bandwidth usage requirement.
- The 16-bit CPU Self-test Library must use less than 2 KB of Program Flash Memory. The library software meets this limit. The actual Program Memory usage is listed in **Chapter 3.3 "Computational Resource Requirements"**.
- The 16-bit CPU Self-test Library must use less than 200 bytes of RAM. The library software meets this limit. The actual Program Memory usage is listed in **Chapter 3.3 "Computational Resource Requirements"**. A common RAM block has been defined for the entire test suite, and varying portions of this block will be utilized by the eight test subsets.
- The 16-bit CPU Self-test Library task may have lower priority than other application tasks. Therefore, each test subset has been designed to include context save and restore of all Special Function Registers (SFRs) used by the function. Some of these registers, W0-W7, are "caller-saved", meaning these SFRs are automatically saved by the C compiler if the function being called uses any of them.

1.2 SOFTWARE PACKAGE FILES

The files in the 16-bit CPU Self-test Library software package are:

1.2.1 CpuTestSubsets.s

This is the main assembly language source file that contains all eight test subset functions. Each function is defined as a C-callable Assembly subroutine with no input parameters and a 16-bit return value.

1.2.2 CpuTestISR.s

This Assembly language source file contains all interrupt and trap service routines used by the test subset functions to test some interrupt-related features such as math error traps and the `DISI` instruction. These handlers are utilized by multiple test subset routines, and are defined to use the Alternate Interrupt Vector Table (AIVT).

1.2.3 CPUverification.inc

This Assembler include file contains several definitions that are shared by all of the test subset functions:

- Definitions for program Flash memory and data RAM sizes. The correct memory sizes must be defined by the user based on the device being tested. In the example application projects for the five devices included in the software package, the device memory size is predefined in this file.
- Definitions of constants stored in program Flash memory, for testing Program Space Visibility (PSV) and table reads in test subset 2.
- Definitions of RAM variables and arrays used by all of the test subset functions
- Definitions of various constants used by various test subsets.

Note: If the device being tested has a program Flash memory size and/or RAM size that is different from the options provided in this file, the addresses of the constants and/or variables in this file would need to be customized by the user.

1.2.4 Application.c

This file is an example user application demonstrating how the test subset functions can be executed by an application in real-time. A 16-bit general-purpose timer (Timer2) and a case-switching statement are utilized by the application to call a different test subset every 2 ms. This sequence ensures that the entire test-suite has been completely executed within a 16 ms window. The returned test results (6 or 8, depending on whether a PIC24H/PIC24E or a dsPIC33F/dsPIC33E device is being used) are stored in an array named *TestResults*, and may be inspected in a Watch window using debugging tools such as MPLAB ICD 3 or MPLAB REAL ICE™. The user application logs the results in an array.

1.2.5 Example Application Projects

MPLAB IDE project files are included in the software package for the following five devices:

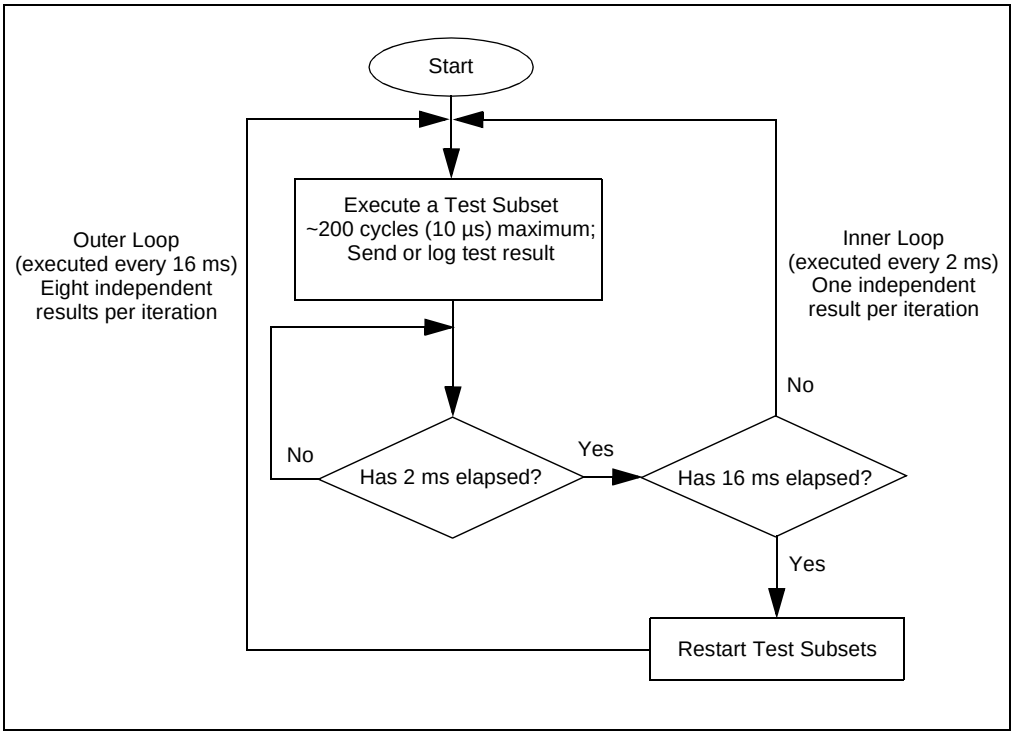
- dsPIC33FJ256GP710A
- dsPIC33EP64MC506
- dsPIC33EP512MU810
- PIC24HJ256GP610A
- PIC24EP512GU810

NOTES:

Chapter 2. Algorithm Flow

The general execution flow of the CPU Self-Test Library is illustrated in Figure 2-1.

FIGURE 2-1: CPU SELF-TEST LIBRARY ALGORITHM EXECUTION FLOW



The overall test suite is sub-divided into eight test subset functions, which are executed in a cyclic manner. A different test subset function is called by the application every 2 ms, thereby completing the entire test suite every 16 ms. Since each test subset generates a unique 16-bit data result, eight such test results (each representing a different subset of CPU functionality) are generated during the 16 ms window.

A separate C-callable function is provided for each test subset. Also, all functionality specific to dsPIC33F/dsPIC33E (i.e., features that are not present in the PIC24H/PIC24E architecture) is tested only in test subsets 7 and 8, making the test suite highly modular.

An overview of each test suite is provided in **Chapter 3. "Test Software Subsets"**.

NOTES:

Chapter 3. Test Software Subsets

The 16-bit CPU Self-test Library software is divided into eight test subsets. Each of the test subsets validates several features and components of the CPU. Each subset is designed in such a way that the result of one operation is used as a source operand for the next instruction. In some cases, different sets of operations on the same original seed value yield different intermediate results, which are then combined within the same test subset function using arithmetic operations such as ADD and logical operations such as XOR. Therefore, there is a sequential dependency between various operations tested with a test subset, and a failure of any feature tested in a test subset is manifested by the generation of an incorrect final 16-bit result generated by that test subset (and interpreted by the secondary processor as being incorrect).

3.1 TEST SUBSET RESULTS

Each test subset is a C-callable Assembly function, and returns the 16-bit result generated by the test subset. The calling function can then either log this 16-bit value or transmit it to a secondary processor through a suitable communication interface such as SPI. The expected 16-bit results that would indicate correct CPU functionality are listed in Table 3-1 for two representative devices from the PIC24H and dsPIC33F, and also for three representative devices from the PIC24E and dsPIC33E families. Note that test subset 2 and subset 7 results depend on the specific device on which the test is being executed, for two reasons:

1. Device ID reads are used to test reads of Configuration memory space (test subset 2 only).
2. Some of the program Flash and data RAM read/writes tests include some accesses of memory addresses that are not present on all devices. The include file `CPUverification.inc` contains preprocessor definitions for Flash and RAM sizes, that the user can customize based on the specific device used.

TABLE 3-1: EXPECTED 16-BIT CPU FUNCTIONALITY RESULTS

Test Subset	Expected Result				
	PIC24HJ256GP610A	dsPIC33FJ256GP710A	dsPIC33EP64MC506	PIC24EP512GU810	dsPIC33EP512MU810
1	0x694D	0x694D	0x694D	0x694D	0x694D
2	0x5F7F	0x6003	0xCE7E	0x743A	0x7476
3	0xC2A7	0xC2A7	0xC2AB	0xC2AB	0xC2AB
4	0x00F8	0x00F8	0x00F8	0x00F8	0x00F8
5	0x1BD2	0x1BD2	0x1BD2	0x1BD2	0x1BD2
6	0xAE40	0xAE40	0xAE40	0xAE40	0xAE40
7	N/A	0xE340	0xABA4	N/A	0x7222
8	N/A	0x1D7D	0x1D7D	N/A	0x1D7D

3.2 TEST SUBSET DESCRIPTIONS

This section provides a brief description of the key features tested in each of the eight test subsets.

3.2.1 Subset 1

Test Subset 1 performs the following basic operations:

- All of the Move instructions are tested
- The addressing modes tested are:
  - Immediate
  - File register
  - Register direct and indirect (with pre-increment, post-increment, pre-decrement, post-decrement, literal offset, and register offset)
- SWAP and EXCH instructions are tested
- All bit-manipulation, bit-test and bit-compare-skip operations are tested
- Single-word and double-word instructions are tested
- Byte move instructions are also checked

3.2.2 Subset 2

Test Subset 2 performs the following basic operations:

- PSV and table accesses from different sections (four locations) of program memory
- All bits of the program memory Address Bus are toggled
- All bits of the data memory Address Bus are toggled
- All bits of the X Data Read and Write Buses are toggled
- CPU registers tested for read/write operations are:
  - W0-W15
  - SPLIM
  - TBLPAG
  - PSVPAG or DSRPAG
- Tested Read after Write (RAW) dependency
- Tested NOP and NOPR instructions

3.2.3 Subset 3

Test Subset 3 performs the following basic operations:

- All conditional branch and GOTO instructions with alternative conditions
- Program Counter (PC) behavior during above program flow change operations
- All Call and Return operations
- Automatic context save on stack
- All Stack and Shadow operations
- DISI instruction.

3.2.4 Subset 4

Test Subset 4 performs the following basic operations:

- Branch instructions tested for false condition are NOV, Z, NN, NC, and NZ
- All logic instructions: AND, CLR, COM, IOR, NEG, SETM and XOR Instructions
- All data rotate and shift instructions
- All compare and compare-skip instructions
- The Z, OV, DC, N, and C bits of the status register are checked for their behavior
- Some byte-mode logic instructions are tested

3.2.5 Subset 5

Test Subset 5 performs the following basic operations:

- The following instructions are tested:
  - ADD
  - ADDC
  - SUB
  - SUBB
  - SUBBR
  - INC
  - INC2
  - DEC
  - DEC2
  - SE
  - ZE
- The addressing modes tested here are:
  - Immediate
  - File register
  - Register direct
- Byte instructions are also checked
- Branch instructions tested for true condition are:
  - GT
  - GTU
  - LE
  - LEU
  - NC
  - NN
  - OV
- Branch instructions tested for false condition are:
  - C
  - GE
  - GEU
  - LT
  - LTU
  - N
  - NOV
- Divide Unsigned Double (DIV.UD) instruction is tested

3.2.6 Subset 6

Test Subset 6 performs the following basic operations:

- All MUL instruction variants
- All DIV instruction variants except DIVF and DIV.UD
- REPEAT loop
- Math error trap generation (divide-by-zero error)

3.2.7 Subset 7

Test Subset 7 performs the following basic operations:

- All DSP accumulator operations, including different bit states of the individual bits of both accumulators
- All DSP multiplier-based instructions
- All DSP MAC register indirect addressing modes
- All DSP shift instructions
- Math error trap generation due to accumulator-related events (accumulator overflow and catastrophic overflow)
- CORCON bit behavior

3.2.8 Subset 8

Test Subset 8 performs the following basic operations:

- Modulo Addressing (both byte and word modes)
- Bit-reversed Addressing
- `DO` loop
- Fractional Divide (`DIVF`) instruction

3.3 COMPUTATIONAL RESOURCE REQUIREMENTS

The instruction cycle counts, RAM requirements and program Flash memory requirements of all eight Test Subset functions for five devices are listed in Table 3-2 through Table 3-6.

All RAM and Flash requirements are within the targeted maximum limits of 200 bytes and 2 KB (2048 bytes), respectively.

TABLE 3-2: RESOURCE REQUIREMENTS FOR THE PIC24HJ256GP610A DEVICE

Test Subset	Instruction Cycles(3)	RAM (bytes)	Flash (bytes)
1	98	6	246
2	105	34	273
3	114	80	300
4	98	4	279
5	104	2	249
6	116	14	156(4)
7	N/A	N/A	N/A
8	N/A	N/A	N/A
Total	635	120(1,2)	1503

Note 1: In addition, a minimum stack size of 98 bytes must be specified in the Linker settings, to support the execution of the 16-bit CPU Self-test Library routines.

2: A total (non-contiguous) RAM space of up to 26 bytes is reserved for all constants and variables, and the stack used by all the CPU-self test routines.

3: The instruction cycle counts listed here include the instruction cycles required by the `CALL` and `RETURN` instructions for each function call, as well as the cycles needed to save and restore the registers used in these functions.

4: The Flash memory usage listed for this test subset includes an Interrupt Service Routine that is shared between test subsets 6 and 7.

TABLE 3-3: RESOURCE REQUIREMENTS FOR THE PIC24EP512GU810 DEVICE

Test Subset	Instruction Cycles(3)	RAM (bytes)	Flash (bytes)
1	105	6	246
2	131	34	267
3	173	78	300
4	105	4	279
5	125	2	249
6	135	12	147(4)
7	N/A	N/A	N/A
8	N/A	N/A	N/A
Total	774	118(1,2)	1488

Note 1: In addition, a minimum stack size of 98 bytes must be specified in the Linker settings, to support the execution of the 16-bit CPU Self-test Library routines.

2: A total (non-contiguous) RAM space of up to 26 bytes is reserved for all constants and variables, and the stack used by all the CPU-self test routines.

3: The instruction cycle counts listed here include the instruction cycles required by the `CALL` and `RETURN` instructions for each function call, as well as the cycles needed to save and restore the registers used in these functions.

4: The Flash memory usage listed for this test subset includes an Interrupt Service Routine that is shared between test subsets 6 and 7.

TABLE 3-4: RESOURCE REQUIREMENTS FOR THE dsPIC33FJ256GP710A DEVICE

Test Subset	Instruction Cycles(3)	RAM (bytes)	Flash (bytes)
1	98	6	246
2	105	34	273
3	114	80	300
4	98	4	279
5	104	2	249
6	116	14	156(4)
7	130	44	288
8	131	42	246
Total	896	124(1,2)	2037

Note 1: In addition, a minimum stack size of 98 bytes must be specified in the Linker settings, to support the execution of the 16-bit CPU Self-test Library routines.

2: A total (non-contiguous) RAM space of up to 26 bytes is reserved for all constants and variables, and the stack used by all the CPU-self test routines.

3: The instruction cycle counts listed here include the instruction cycles required by the `CALL` and `RETURN` instructions for each function call, as well as the cycles needed to save and restore the registers used in these functions.

4: The Flash memory usage listed for this test subset includes an Interrupt Service Routine that is shared between test subsets 6 and 7.

TABLE 3-5: RESOURCE REQUIREMENTS FOR THE dsPIC33EP512MU810 DEVICE

Test Subset	Instruction Cycles(3)	RAM (bytes)	Flash (bytes)
1	105	6	246
2	131	34	267
3	173	78	300
4	105	4	279
5	125	2	249
6	135	12	147(4)
7	177	44	279
8	144	42	246
Total	1095	124(1,2)	2013

Note 1: In addition, a minimum stack size of 98 bytes must be specified in the Linker settings, to support the execution of the 16-bit CPU Self-test Library routines.

2: A total (non-contiguous) RAM space of up to 26 bytes is reserved for all constants and variables, and the stack used by all the CPU-self test routines.

3: The instruction cycle counts listed here include the instruction cycles required by the `CALL` and `RETURN` instructions for each function call, as well as the cycles needed to save and restore the registers used in these functions.

4: The Flash memory usage listed for this test subset includes an Interrupt Service Routine that is shared between test subsets 6 and 7.

TABLE 3-6: RESOURCE REQUIREMENTS FOR THE dsPIC33EP64MC506 DEVICE

Test Subset	Instruction Cycles(3)	RAM (bytes)	Flash (bytes)
1	105	6	246
2	111	30	219
3	173	78	300
4	105	4	279
5	125	2	249
6	135	12	147(4)
7	177	44	279
8	144	42	246
Total	1075	120(1,2)	1965

Note 1: In addition, a minimum stack size of 98 bytes must be specified in the Linker settings, to support the execution of the 16-bit CPU Self-test Library routines.

2: A total (non-contiguous) RAM space of up to 26 bytes is reserved for all constants and variables, and the stack used by all the CPU-self test routines.

3: The instruction cycle counts listed here include the instruction cycles required by the `CALL` and `RETURN` instructions for each function call, as well as the cycles needed to save and restore the registers used in these functions.

4: The Flash memory usage listed for this test subset includes an Interrupt Service Routine that is shared between test subsets 6 and 7.

NOTES:

Chapter 4. Functional Test Coverage

4.1 INSTRUCTION SET

The instruction classes tested by the CPU Self-Test Library include the types of instructions:

- Data Move
- Program Flow Change
- Stack/Shadow
- Control
- Math
- Logic
- Rotate/Shift
- Compare/Skip
- DSP

Table 4-1 lists all of the instruction variants (each having its own op code) supported by the 16-bit instruction set, along with the index of the first test subset that exercised and tested the functionality of the instruction.

Note: All instructions tested in test subsets 7 and 8 are those that are supported by the dsPIC33F/dsPIC33E only, and are not supported by the PIC24H/PIC24E devices. These DSP operations have been listed under various other instruction classes based on their functionality.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Instruction Class – MOVE				
EXCH	Wns, Wnd	X	X	1
MOV	f	X	X	1
MOV	f, Wreg	X	X	1
MOV	Wreg, f	X	X	1
MOV	f, Wnd	X	X	1
MOV	Wns, f	X	X	1
MOV.b	#Lit8, Wnd	X	X	1
MOV	#Lit16, Wnd	X	X	1
MOV	[Ws+Slit10], Wnd	X	X	1
MOV	Wns, [Ws+SLit10]	X	X	1
MOV	Ws, Wd	X	X	1
MOV.D	Ws, Wnd	X	X	1
MOV.D	Wns, Wd	X	X	1
MOVPAG	#lit0, DSRPAG	X(1)	X(1)	2
MOVPAG	#lit7, DSWPAG	X(1)	X(1)	2
MOVPAG	#lit8, TBLPAG	X(1)	X(1)	2
MOVPAG	Wn, DSRPAG	X(1)	X(1)	2
MOVPAG	Wn, DSWPAG	X(1)	X(1)	2
MOVPAG	Wn, TBLPAG	X(1)	X(1)	2
SWAP	Wn	X	X	1
TBLRDH	Ws, Wd	X	X	2
TBLRDL	Ws, Wd	X	X	2
TBLWTH	Ws, Wd	X	X	N/A
TBLWTL	Ws, Wd	X	X	N/A
MOVAC	Acc, Wx, Wxd, Wy, Wyd, AWB	N/A	X	7
SAC	Acc, #SLit4, Wdo	N/A	X	7
SAC.R	Acc, #SLit4, Wdo	N/A	X	7
LAC	Wso, #SLit4, Acc	N/A	X	7
Instruction Class – BIT				
BCLR	f, #bit4	X	X	3
BCLR	Ws, #bit4	X	X	1
BSET	f, #bit4	X	X	1
BSET	Ws, #bit4	X	X	1
BSW.C	Ws, Wb	X	X	1
BSW	Ws, Wb	X	X	1
BTG	f, #bit4	X	X	1
BTG	Ws, #bit4	X	X	1
BTST	f, #bit4	X	X	1
BTST.C	Ws, #bit4	X	X	1
BTST.Z	Ws, #bit4	X	X	1

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
BTST.C	Ws, Wb	X	X	1
BTST.Z	Ws, Wb	X	X	1
BTSTS	f, #bit4	X	X	1
BTSTS.C	Ws, #bit4	X	X	1
BTSTS.Z	Ws, #bit4	X	X	1
FBCL	Ws, Wnd	X	X	1
FFIL	Ws, Wnd	X	X	1
FFIR	Ws, Wnd	X	X	1
Instruction Class – MATH				
ADD	f, Wreg	X	X	3
ADD	f	X	X	5
ADD	#Lit10, Wn	X	X	3
ADD	Wb, #Lit5, Wd	X	X	5
ADD	Wb, Ws, Wd	X	X	3
ADD	Acc	N/A	X	7
ADD	Wso, #SLit4, Acc	N/A	X	7
ADDC	f, Wreg	X	X	5
ADDC	f	X	X	5
ADDC	#Lit10, Wn	X	X	5
ADDC	Wb, Ws, Wd	X	X	5
ADDC	Wb, #Lit5, Wd	X	X	5
DAW.B	Wn	X	X	5
DEC	f	X	X	5
DEC	f, Wreg	X	X	5
DEC	Ws, Wd	X	X	3
DEC2	f	X	X	5
DEC2	f, Wreg	X	X	5
DEC2	Ws, Wd	X	X	5
DIV.S	Wm, Wn	X	X	6
DIV.SD	Wm, Wn	X	X	6
DIV.U	Wm, Wn	X	X	6
DIV.UD	Wm, Wn	X	X	5
DIVF	Wm, Wn	X	X	8
INC	f	X	X	5
INC	f, Wreg	X	X	5
INC	Ws, Wd	X	X	5
INC2	f	X	X	5
INC2	f, Wreg	X	X	5
INC2	Ws, Wd	X	X	5
MUL	f	X	X	6
MUL.SS	Wb, Ws, Wd/Acc(2)	X	X	5
MUL.SU	Wb,#Lit5, Wnd/Acc(2)	X	X	5

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
MUL.SU	Wb, Ws, Wnd/Acc(2)	X	X	5
MUL.US	Wb, Ws, Wnd/Acc(2)	X	X	5
MUL.UU	Wb,#Lit5, Wnd/Acc(2)	X	X	5
MUL.UU	Wb, Ws, Wnd/Acc(2)	X	X	5
MULW.SS	Wb, Ws, Wnd	X(1)	X(1)	—
MULW.SU	Wb, Ws, Wnd	X(1)	X(1)	—
MULW.SU	Wb, #lit5, Wnd	X(1)	X(1)	—
MULW.US	Wb, Ws, Wnd	X(1)	X(1)	—
MULW.UU	Wb, Ws, Wnd	X(1)	X(1)	—
MULW.UU	Wb, #lit5, Wnd	X(1)	X(1)	—
MPY	Wm*Wn, Acc, Wxd, Wy, Wyd	N/A	X	7
MPY	Wm*Wm, Acc, Wxd, Wy, Wyd	N/A	X	7
MPY.N	Wm*Wn, Acc, Wxd, Wy, Wyd	N/A	X	7
MSC	Wm*Wm, Acc, Wxd, Wy, Wyd, AWB	N/A	X	7
MAC	Wm*Wm, Acc, Wxd, Wy, Wyd, AWB	N/A	X	7
MAC	Wm*Wn, Acc, Wxd, Wy, Wyd, AWB	N/A	X	7
SE	Ws, Wnd	X	X	5
SUB	f, Wreg	X	X	5
SUB	#Lit10, Wn	X	X	5
SUB	Wb, #Lit5, Wd	X	X	5
SUB	Wb, Ws, Wd	X	X	4
SUB	Acc	N/A	X	7
SUB	f	X	X	5
SUBB	f, Wreg	X	X	5
SUBB	#Lit10, Wn	X	X	5
SUBB	Wb, #Lit5, Wd	X	X	5
SUBB	Wb, Ws, Wd	X	X	5
SUBB	f	X	X	5
SUBBR	f, Wreg	X	X	5
SUBBR	Wb, #Lit5, Wd	X	X	5
SUBBR	Wb, Ws, Wd	X	X	5
SUBBR	f	X	X	5
SUBR	f, Wreg	X	X	5
SUBR	Wb, #Lit5, Wd	X	X	5
SUBR	Wb, Ws, Wd	X	X	5
SUBR	f	X	X	5
ZE	Ws, Wnd	X	X	5
ED	Wm*Wm, Acc, Wx, Wy, Wxd	N/A	X	7
EDAC	Wm*Wm, Acc, Wx, Wy, Wxd	N/A	X	7

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Instruction Class – LOGIC				
AND	f, Wreg	X	X	3
AND	#Lit10, Wn	X	X	4
AND	Wb, #Lit5, Wd	X	X	4
AND	Wb, Ws, Wd	X	X	4
AND	f	X	X	1
CLR	f	X	X	4
CLR	Wreg	X	X	3
CLR	Wd	X	X	4
CLR	Acc, Wx, Wxd, Wy, Wyd, AWB	N/A	X	7
COM	f	X	X	4
COM	f, Wreg	X	X	4
COM	Ws, Wd	X	X	4
IOR	f	X	X	4
IOR	f, Wreg	X	X	4
IOR	#Lit10, Wn	X	X	4
IOR	Wb, #Lit5, Wd	X	X	4
IOR	Wb, Ws, Wd	X	X	4
NEG	f	X	X	4
NEG	f, Wreg	X	X	4
NEG	Ws, Wd	X	X	4
NEG	Acc	N/A	X	7
SETM	f	X	X	4
SETM	Wreg	X	X	4
SETM	Wd	X	X	4
XOR	f	X	X	4
XOR	f, Wreg	X	X	4
XOR	#Lit10, Wn	X	X	4
XOR	Wb, #Lit5, Wd	X	X	4
XOR	Wb, Ws, Wd	X	X	4
Instruction Class – ROTATE/SHIFT				
ASR	f, Wreg	X	X	4
ASR	Ws, Wd	X	X	4
ASR	Wb, #Lit4, Wnd	X	X	4
ASR	Wb, Wns, Wnd	X	X	4
ASR	f	X	X	4
LSR	f, Wreg	X	X	4
LSR	Ws, Wd	X	X	4
LSR	Wb, #Lit4, Wnd	X	X	4
LSR	Wb, Wns, Wnd	X	X	4
LSR	f	X	X	4

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
RLC	f, Wreg	X	X	4
RLC	Ws, Wd	X	X	4
RLC	f	X	X	4
RLNC	f, Wreg	X	X	4
RLNC	Ws, Wd	X	X	4
RLNC	f	X	X	4
RRC	f, Wreg	X	X	4
RRC	Ws, Wd	X	X	4
RRC	f	X	X	4
RRNC	f, Wreg	X	X	4
RRNC	Ws, Wd	X	X	4
RRNC	f	X	X	4
SL	f, Wreg	X	X	4
SL	Ws,Wd	X	X	4
SL	Wb, #Lit4, Wnd	X	X	4
SL	Wb, Wns, Wnd	X	X	4
SL	f	X	X	4
SFTAC	Acc, Wn	N/A	X	7
SFTAC	Acc, #SLit6	N/A	X	7
Instruction Class – COMPARE/SKIP				
BTSC	f, #bit4	X	X	1
BTSC	Ws, #bit4	X	X	1
BTSS	f, #bit4	X	X	1
BTSS	Ws, #bit4	X	X	1
CP	f	X	X	4
CP	Wb, #Lit5	X	X	4
CP	Wb, Ws	X	X	4
CP0	f	X	X	4
CP0	Ws	X	X	4
CPB	f	X	X	4
CPB	Wb, #Lit5	X	X	4
CPB	Wb, Ws	X	X	4
CPBEQ	Wb, Wn, Expr	X(1)	X(1)	—
CPBGT	Wb, Wn, Expr	X(1)	X(1)	—
CPBLT	Wb, Wn, Expr	X(1)	X(1)	—
CPBNE	Wb, Wn, Expr	X(1)	X(1)	—
CPSEQ	Wb, Ws	X	X	4
CPSGT	Wb, Wn	X	X	4
CPSLT	Wb, Wn	X	X	4
CPSNE	Wb, Wn	X	X	4

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Instruction Class – PROGRAM FLOW				
BRA	Expr	X	X	3
BRA	Wn	X	X	3
BRA	C, Expr	X	X	3
BRA	GE, Expr	X	X	3
BRA	GEU, Expr	X	X	3
BRA	GT, Expr	X	X	3
BRA	GTU, Expr	X	X	3
BRA	LE, Expr	X	X	3
BRA	LEU, Expr	X	X	3
BRA	LT, Expr	X	X	3
BRA	LTU, Expr	X	X	3
BRA	N, Expr	X	X	3
BRA	NC, Expr	X	X	3
BRA	NN, Expr	X	X	3
BRA	NOV, Expr	X	X	3
BRA	NZ, Expr	X	X	3
BRA	OA, Expr	N/A	X	7
BRA	OB, Expr	N/A	X	7
BRA	OV, Expr	X	X	3
BRA	SA, Expr	N/A	X	7
BRA	SB, Expr	N/A	X	7
BRA	Z, Expr	X	X	3
CALL	Expr	X	X	3
CALL	Wn	X	X	3
CALL.L	Wn	X(1)	X(1)	—
GOTO	Expr	X	X	3
GOTO	Wn	X	X	3
GOTO.L	Wn	X(1)	X(1)	—
RCALL	Expr	X	X	3
RCALL	Wn	X	X	3
REPEAT	#Lit14	X	X	5
REPEAT	Wn	X	X	6
RETFIE		X	X	3
RETLW	#Lit10, Wn	X	X	3
RETURN		X	X	3
Instruction Class – SHADOW/STACK				
LNK	#Lit14	X	X	3
POP	f	X	X	3
POP	Wd	X	X	3
POP.D	Wnd	X	X	3

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

TABLE 4-1: SUPPORTED 16-BIT INSTRUCTION SET (CONTINUED)

Instruction Set		Applies To:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
POP.S		X	X	3
PUSH	f	X	X	3
PUSH	Ws	X	X	3
PUSH.D	Wns	X	X	3
PUSH.S		X	X	3
ULNK		X	X	3
Instruction Class – CONTROL				
CLRWDT		X	X	N/A
DISI	#Lit14	X	X	3
NOP		X	X	3
NOPR		X	X	3
PWRSAV	#Lit1	X	X	N/A
RESET		X	X	N/A
DO	#Lit4, Expr	N/A	X	8
DO	Wn, Expr	N/A	X	7

Note 1: This instruction is available in dsPIC33E and PIC24E devices only.

2: Accumulator A or B can used as the destination register in dsPIC33E devices only.

4.1.1 Methodology for Assessing the Functional Test Coverage for CPU Instructions

The entire set of instruction variants were listed in the matrix in Table 4-1 and counted. Then, the instructions tested by at least one test subset were counted based on code inspection. The percentage test coverage is then given by:

```
[(Tested Instructions / Available Instructions)] * 100
```

The only instructions that are not tested are those that disrupt the real-time nature of the application, such as operations that cause a device Reset (`CLRWDT` and `RESET`), reprogram Flash Memory (`TBLWTL` and `TBLWTH`), or put the device in Sleep or Idle mode (`PWRSAV`).

If these five instructions are excluded from the assessment of instruction test coverage, the test coverage for CPU instructions is 100% for dsPIC33F/PIC24H devices and 95.1% for dsPIC33E/PIC24E devices.

4.2 ADDRESSING MODES

The addressing modes tested by the 16-bit CPU Self-test Library include:

- Register Direct Addressing
- File Register (Memory Direct) Addressing
- Register Indirect Addressing
- Register Indirect Addressing with pre-increment
- Register Indirect Addressing with post-increment
- Register Indirect Addressing with pre-decrement
- Register Indirect Addressing with post-decrement
- Register Indirect Addressing with literal offset
- Register Indirect Addressing with register offset
- Immediate Addressing
- Program Space Visibility (PSV)
- Table Addressing
- DSP Register Indirect with special post-increment/post-decrement and register offset modes (dsPIC33F/dsPIC33E only)
- Modulo Addressing (dsPIC33F/dsPIC33E only)
- Bit-reversed Addressing (dsPIC33F/dsPIC33E only)

Data widths that are supported by the CPU are Byte (8 bits), Word (16 bits), and Double-word (32 bits). Each of these have been explicitly tested.

Table 4-2 lists all of the addressing modes supported by the 16-bit architecture, along with the index of the first test subset that exercised and tested the functionality of the instruction.

Note: All addressing modes tested in test subsets 7 and 8 are those that are supported by dsPIC33F/dsPIC33E devices only and are not supported by PIC24H/PIC24E devices.

TABLE 4-2: SUPPORTED 16-BIT ADDRESSING MODES

Addressing Mode		Applies to:		Test Subset Coverage
		PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Register Direct		X	X	1
Memory Direct		X	X	1
Register Indirect	Pre-Increment	X	X	1
	Post-Increment	X	X	1
	Pre-Decrement	X	X	1
	Post-Decrement	X	X	1
	Register Offset	X	X	1
	Literal Offset	X	X	1
	No Modification	X	X	1
Immediate		X	X	1
Byte Addressing		X	X	1
Double-word Addressing		X	X	1
PSV		X	X	2
Table		X	X	2
MAC Register Indirect	Post-Increment by 2	N/A	X	7
	Post-Increment by 4	N/A	X	7
	Post-Increment by 6	N/A	X	7
	Post-Decrement by 2	N/A	X	7
	Post-Decrement by 4	N/A	X	7
	Post-Decrement by 6	N/A	X	7
	Register Offset (Indexed)	N/A	X	7
	No Modification	N/A	X	7
Accumulator Write Back	Direct Addressing	N/A	X	7
	Indirect with Post-Increment	N/A	X	7
Modulo Addressing (Byte Mode)		N/A	X	8
Modulo Addressing (Word Mode)		N/A	X	8
Bit Reversed Addressing		N/A	X	8

4.2.1 Methodology for Assessing the Functional Test Coverage for CPU Addressing Modes

The entire set of addressing mode variants were listed in the matrix in Table 4-1 and counted. Then, the addressing modes tested by at least one test subset were counted based on code inspection. The percentage test coverage is then given by:

```
[(Tested Addressing Modes / Available Addressing Modes)] * 100
```

The test coverage for CPU addressing modes is 100% ([(27/27)*100]).

4.3 CPU REGISTERS

The SFRs tested by the 16-bit CPU Self-test Library include:

- Working Registers (W0 through W15)
- Stack Pointer Limit Register (SPLIM)
- Table Page Register (TBLPAG)
- Program Space Visibility Page Register (PSVPAG) (dsPIC33F/PIC24H only) or Data Space Read Page Register (DSRPAG) (dsPIC33E/PIC24E only)
- Core Control Register (CORCON)
- CPU Status Register (SR)
- Interrupt Control Register 2 (INTCON2)
- Modulo Addressing Control Register (MODCON) (dsPIC33F/dsPIC33E only)
- X-RAM Modulo Buffer Start Address Register (dsPIC33F/dsPIC33E only)
- X-RAM Modulo Buffer End Address Register (dsPIC33F/dsPIC33E only)
- Y-RAM Modulo Buffer Start Address Register (dsPIC33F/dsPIC33E only)
- Y-RAM Modulo Buffer End Address Register (dsPIC33F/dsPIC33E only)
- Bit-reversed Addressing Control Register (XBREV) (dsPIC33F/dsPIC33E only)

Each control bit present in the above registers has been exercised and tested for both set (‘1’) and clear (‘0’) states.

Table 4-3 lists all of the CPU-related registers in the 16-bit architecture, including the bits present therein, along with the test subset that first exercised each.

Note: All registers or bits tested in test subsets 7 and 8 are those that are supported by dsPIC33F/dsPIC33E devices only and are not supported by PIC24H/PIC24E devices.

TABLE 4-3: SUPPORTED 16-BIT CPU REGISTERS

Register Name	Bit Number	Bit Name	Applies To:		Test Subset Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
W0	—	—	X	X	1
W1	—	—	X	X	1
W2	—	—	X	X	1
W3	—	—	X	X	1
W4	—	—	X	X	1
W5	—	—	X	X	1
W6	—	—	X	X	1
W7	—	—	X	X	1
W8	—	—	X	X	2
W9	—	—	X	X	2
W10	—	—	X	X	2
W11	—	—	X	X	2
W12	—	—	X	X	2
W13	—	—	X	X	2
W14	—	—	X	X	2
W15	—	—	X	X	2
SPLIM	—	—	X	X	2
TBLPAG	—	—	X	X	2
PSVPAG or DSRPAG	—	—	X	X	2
DSWPAG (dsPIC33E/PIC24E)	—	—	X	X	-
CORCON	bit 0	IF	N/A	X	7
	bit 1	RND	N/A	X	7
	bit 2	PSV or SFA	X	X	2 (PSV only)
	bit 3	IPL3	X	X	6
	bit 4	ACCSAT	N/A	X	7
	bit 5	SATDW	N/A	X	7
	bit 6	SATB	N/A	X	7
	bit 7	SATA	N/A	X	7
	bit 8-10	DL	N/A	X	7
	bit 11	EDT	N/A	X	7
	bit 12	US	N/A	X	7
	bit 13-15	Unimplemented	N/A	N/A	N/A

TABLE 4-3: SUPPORTED 16-BIT CPU REGISTERS (CONTINUED)

Register Name	Bit Number	Bit Name	Applies To:		Test Subset Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
SR	bit 0	C	X	X	2
	bit 1	Z	X	X	2
	bit 2	OV	X	X	2
	bit 3	N	X	X	2
	bit 4	RA	X	X	5
	bit 7-5	IPL	X	X	3
	bit 8	DC	X	X	5
	bit 9	DA	N/A	X	7
	bit 10	SAB	N/A	X	7
	bit 11	OAB	N/A	X	7
	bit 12	SB	N/A	X	7
	bit 13	SA	N/A	X	7
	bit 14	OB	N/A	X	7
	bit 15	OA	N/A	X	7
INTCON2	bit 0	INT0EP	X	X	N/A
	bit 1	INT1EP	X	X	N/A
	bit 2	INT2EP	X	X	N/A
	bit 3	INT3EP	X	X	N/A
	bit 4	INT4EP	X	X	N/A
	bit 5-13	Unimplemented	N/A	N/A	N/A
	bit 14	DISI	X	X	3
	bit 15	ALTIVT	X	X	3
MODCON	bits 0-3	XWM	X	X	8
	bits 4-7	YWM	N/A	X	8
	bits 8-11	BWM	N/A	X	8
	bits 12-13	Unimplemented	N/A	N/A	N/A
	bit 14	YMODEN	N/A	X	8
	bit 15	XMODEN	X	X	8
XMODSRT	—	—	X	X	8
XMODEND	—	—	X	X	8
YMODSRT	—	—	N/A	X	8
YMODEND	—	—	N/A	X	8
XBREV	bits 0-14	BWM	N/A	X	8
	bit 15	BREN	N/A	X	8
ACCA	bit 39	—	N/A	X	7
	bit 38	—	N/A	X	7
	bit 37	—	N/A	X	7
	bit 36	—	N/A	X	7
	bit 35	—	N/A	X	7
	bit 34	—	N/A	X	7
	bit 33	—	N/A	X	7
	bit 32	—	N/A	X	7
	bit 31	—	N/A	X	7

TABLE 4-3: SUPPORTED 16-BIT CPU REGISTERS (CONTINUED)

Register Name	Bit Number	Bit Name	Applies To:		Test Subset Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
ACCA	bit 30	—	N/A	X	7
	bit 29	—	N/A	X	7
	bit 28	—	N/A	X	7
	bit 27	—	N/A	X	7
	bit 26	—	N/A	X	7
	bit 25	—	N/A	X	7
	bit 24	—	N/A	X	7
	bit 23	—	N/A	X	7
	bit 22	—	N/A	X	7
	bit 21	—	N/A	X	7
	bit 20	—	N/A	X	7
	bit 19	—	N/A	X	7
	bit 18	—	N/A	X	7
	bit 17	—	N/A	X	7
	bit 16	—	N/A	X	7
	bit 15	—	N/A	X	7
	bit 14	—	N/A	X	7
	bit 13	—	N/A	X	7
	bit 12	—	N/A	X	7
	bit 11	—	N/A	X	7
	bit 10	—	N/A	X	7
	bit 9	—	N/A	X	7
	bit 8	—	N/A	X	7
	bit 7	—	N/A	X	7
	bit 6	—	N/A	X	7
	bit 5	—	N/A	X	7
	bit 4	—	N/A	X	7
	bit 3	—	N/A	X	7
	bit 2	—	N/A	X	7
	bit 1	—	N/A	X	7
	bit 0	—	N/A	X	7
ACCB	bit 39	—	N/A	X	7
	bit 38	—	N/A	X	7
	bit 37	—	N/A	X	7
	bit 36	—	N/A	X	7
	bit 35	—	N/A	X	7
	bit 34	—	N/A	X	7
	bit 33	—	N/A	X	7
	bit 32	—	N/A	X	7
	bit 31	—	N/A	X	7
	bit 30	—	N/A	X	7
	bit 29	—	N/A	X	7
	bit 28	—	N/A	X	7
	bit 27	—	N/A	X	7

TABLE 4-3: SUPPORTED 16-BIT CPU REGISTERS (CONTINUED)

Register Name	Bit Number	Bit Name	Applies To:		Test Subset Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
ACCB	bit 26	—	N/A	X	7
	bit 25	—	N/A	X	7
	bit 24	—	N/A	X	7
	bit 23	—	N/A	X	7
	bit 22	—	N/A	X	7
	bit 21	—	N/A	X	7
	bit 20	—	N/A	X	7
	bit 19	—	N/A	X	7
	bit 18	—	N/A	X	7
	bit 17	—	N/A	X	7
	bit 16	—	N/A	X	7
	bit 15	—	N/A	X	7
	bit 14	—	N/A	X	7
	bit 13	—	N/A	X	7
	bit 12	—	N/A	X	7
	bit 11	—	N/A	X	7
	bit 10	—	N/A	X	7
	bit 9	—	N/A	X	7
	bit 8	—	N/A	X	7
	bit 7	—	N/A	X	7
	bit 6	—	N/A	X	7
	bit 5	—	N/A	X	7
	bit 4	—	N/A	X	7
	bit 3	—	N/A	X	7
	bit 2	—	N/A	X	7
	bit 1	—	N/A	X	7
	bit 0	—	N/A	X	—

4.3.1 Methodology for Assessing the Functional Test Coverage for CPU Registers and Bits

The entire set of CPU-related registers, and any individual bits therein, were listed in the matrix and counted. For registers such as XMODSRT, for which the individual bits are not relevant, only the registers are listed and counted. Then, the registers (or wherever applicable, register bits) tested by at least one test subset were counted based on code inspection. The percentage test coverage is then given by:

[(*Tested Registers or Bits* / *Available Registers or Bits*)] * 100

The test coverage for CPU registers is 99.3% ([(134/135)*100])for dsPIC33F/PIC24H devices and 98.5% ([(133/135)*100]) for dsPIC33E/PIC24E devices.

4.4 BUS STRUCTURES

The bus structures tested by the 16-bit CPU Self-test Library include:

- Program Memory Address
- Program Memory Data Read
- X Data Memory Read Address
- X Data Memory Read Data
- X Data Memory Write Address
- X Data Memory Write Data
- Y Data Memory Read Address
- Y Data Memory Read Data

Each bit present in the buses listed above has been exercised and tested for both set ('1') and clear ('0') states.

Table 4-4 lists all of the bus structures in the 16-bit architecture, including all of the bits present therein, along with the test subset that first exercised each.

> **Note:** All buses tested in test subsets 7 and 8 are those that are supported by dsPIC33F/dsPIC33E devices only and are not supported by PIC24H/PIC24E devices.

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Program Memory Address Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2
	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2
	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Program Memory Address Bus	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2
	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2
	16	0	X	X	2
		1	X	X	2
	17	0	X	X	2
		1	X	X	2
	18	0	X	X	2
		1	X	X	2
	19	0	X	X	2
		1	X	X	2
	20	0	X	X	2
		1	X	X	2
	21	0	X	X	2
		1	X	X	2
	22	0	X	X	2
		1	X	X	2
	23	0	X	X	2
		1	X	X	2
Program Memory Data Read Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2
	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Program Memory Data Read Bus	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2
	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2
	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2
Program Memory Data Write Bus	N/A	N/A	N/A	N/A	N/A
X Data Memory Read Address Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2
	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2
	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2
	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2
	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
X Data Memory Read Data Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2
	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2
	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2
	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2
	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2
X Data Memory Write Address Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
X Data Memory Write Address Bus	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2
	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2
	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2
	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2
X Data Memory Write Data Bus	0	0	X	X	2
		1	X	X	2
	1	0	X	X	2
		1	X	X	2
	2	0	X	X	2
		1	X	X	2
	3	0	X	X	2
		1	X	X	2
	4	0	X	X	2
		1	X	X	2
	5	0	X	X	2
		1	X	X	2
	6	0	X	X	2
		1	X	X	2
	7	0	X	X	2
		1	X	X	2
	8	0	X	X	2
		1	X	X	2
	9	0	X	X	2
		1	X	X	2
	10	0	X	X	2
		1	X	X	2
	11	0	X	X	2
		1	X	X	2
	12	0	X	X	2
		1	X	X	2
	13	0	X	X	2
		1	X	X	2

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
X Data Memory Write Data Bus	14	0	X	X	2
		1	X	X	2
	15	0	X	X	2
		1	X	X	2
Y Data Memory Read Address Bus	0	0	N/A	X	7
		1	N/A	X	7
	1	0	N/A	X	7
		1	N/A	X	7
	2	0	N/A	X	7
		1	N/A	X	7
	3	0	N/A	X	7
		1	N/A	X	7
	4	0	N/A	X	7
		1	N/A	X	7
	5	0	N/A	X	7
		1	N/A	X	7
	6	0	N/A	X	7
		1	N/A	X	7
	7	0	N/A	X	7
		1	N/A	X	7
	8	0	N/A	X	7
		1	N/A	X	7
	9	0	N/A	X	7
		1	N/A	X	7
	10	0	N/A	X	7
		1	N/A	X	7
	11	0	N/A	X	7
		1	N/A	X	7
	12	0	N/A	X	7
		1	N/A	X	7
	13	0	N/A	X	7
		1	N/A	X	7
	14	0	N/A	X	7
		1	N/A	X	7
	15	0	N/A	X	7
		1	N/A	X	7
Y Data Memory Read Data Bus	0	0	N/A	X	7
		1	N/A	X	7
	1	0	N/A	X	7
		1	N/A	X	7
	2	0	N/A	X	7
		1	N/A	X	7
	3	0	N/A	X	7
		1	N/A	X	7
	4	0	N/A	X	7
		1	N/A	X	7

TABLE 4-4: SUPPORTED 16-BIT BUS STRUCTURES (CONTINUED)

Bus Structure	Bit #	State	Applies To:		Test Subject Coverage
			PIC24H/PIC24E	dsPIC33F/dsPIC33E	
Y Data Memory Read Data Bus	5	0	N/A	X	7
		1	N/A	X	7
	6	0	N/A	X	7
		1	N/A	X	7
	7	0	N/A	X	7
		1	N/A	X	7
	8	0	N/A	X	7
		1	N/A	X	7
	9	0	N/A	X	7
		1	N/A	X	7
	10	0	N/A	X	7
		1	N/A	X	7
	11	0	N/A	X	7
		1	N/A	X	7
	12	0	N/A	X	7
		1	N/A	X	7
	13	0	N/A	X	7
		1	N/A	X	7
	14	0	N/A	X	7
		1	N/A	X	7
	15	0	N/A	X	7
		1	N/A	X	7

4.4.1 Methodology for Assessing the Functional Test Coverage for Bus Structures and Bus Bit-lines

The entire set of bus structures, and any individual bits therein, were listed in the matrix and counted for both '0' and '1' conditions. The Program Memory Write Bus was not included in the count as program Flash memory reprogramming operations cannot be exercised due to real-time application constraints. Then, the bus bit-lines tested by at least one test subset were counted based on code inspection. The percentage test coverage is then given by:

[(*Tested Bus Bit States* / *Available Bus Bit States*)] * 100.

The test coverage for bus structures is 100% ([(256/256)*100]).

4.5 CPU HARDWARE UNITS

The CPU hardware units tested by the CPU Self-Test Library include:

- Arithmetic and Logic Unit (ALU)
- Multiplier
- Divider
- Data Shifter
- Stack Control
- Interrupt Controller
- Trap Controller
- Program Memory Control
- Data Memory Control
- Instruction Decoding and Control
- X Read Address Generator Unit
- X Write Address Generator Unit
- Y Read Address Generator Unit (dsPIC33F/dsPIC33E only)
- DSP Adder/Subtractor (dsPIC33F/dsPIC33E only)
- DSP Saturation Logic (dsPIC33F/dsPIC33E only)
- DSP Overflow Logic (dsPIC33F/dsPIC33E only)
- DSP Rounding Logic (dsPIC33F/dsPIC33E only)

Table 4-5 lists each of the CPU hardware modules in the 16-bit architecture, along with all the test subsets that tested them.

> **Note:** All hardware modules tested in test subsets 7 and 8 are those that are supported by dsPIC33F/dsPIC33E devices only and are not supported by PIC24H/PIC24E devices.

TABLE 4-5: SUPPORTED 16-BIT CPU HARDWARE MODULES

Hardware Module		Applies To:		Test Subset Coverage
Item Number (see Figure 4-1 and Figure 4-2)	**Module Name**	**PIC24H/PIC24E**	**dsPIC33F/dsPIC33E**	
1	Arithmetic and Logic Unit (ALU)	X	X	5, 6
2	Multiplier	X	X	6, 7
3	Divider	X	X	5, 6, 8
4	Data Shifter	X	X	4, 7
5	DSP Adder/Subtractor	N/A	X	7
6	DSP Saturation Logic	N/A	X	7
7	DSP Overflow Logic	N/A	X	7
8	DSP Rounding Logic	N/A	X	7
9	Stack Control Logic	X	X	3
10	Interrupt Controller	X	X	3
11	Trap Controller	X	X	6
12	Program Memory Control	X	X	2, 3
13	Data Memory Control	X	X	1, 2
14	Program Memory Data Access	X	X	2
15	Instruction Decoding and Control	X	X	All
16	X Read Address Generator Unit	X	X	2
17	X Write Address Generator Unit	X	X	2
18	Y Read Address Generator Unit	N/A	X	7

4.5.1 Methodology for Assessing the Functional Test Coverage for CPU Hardware Modules

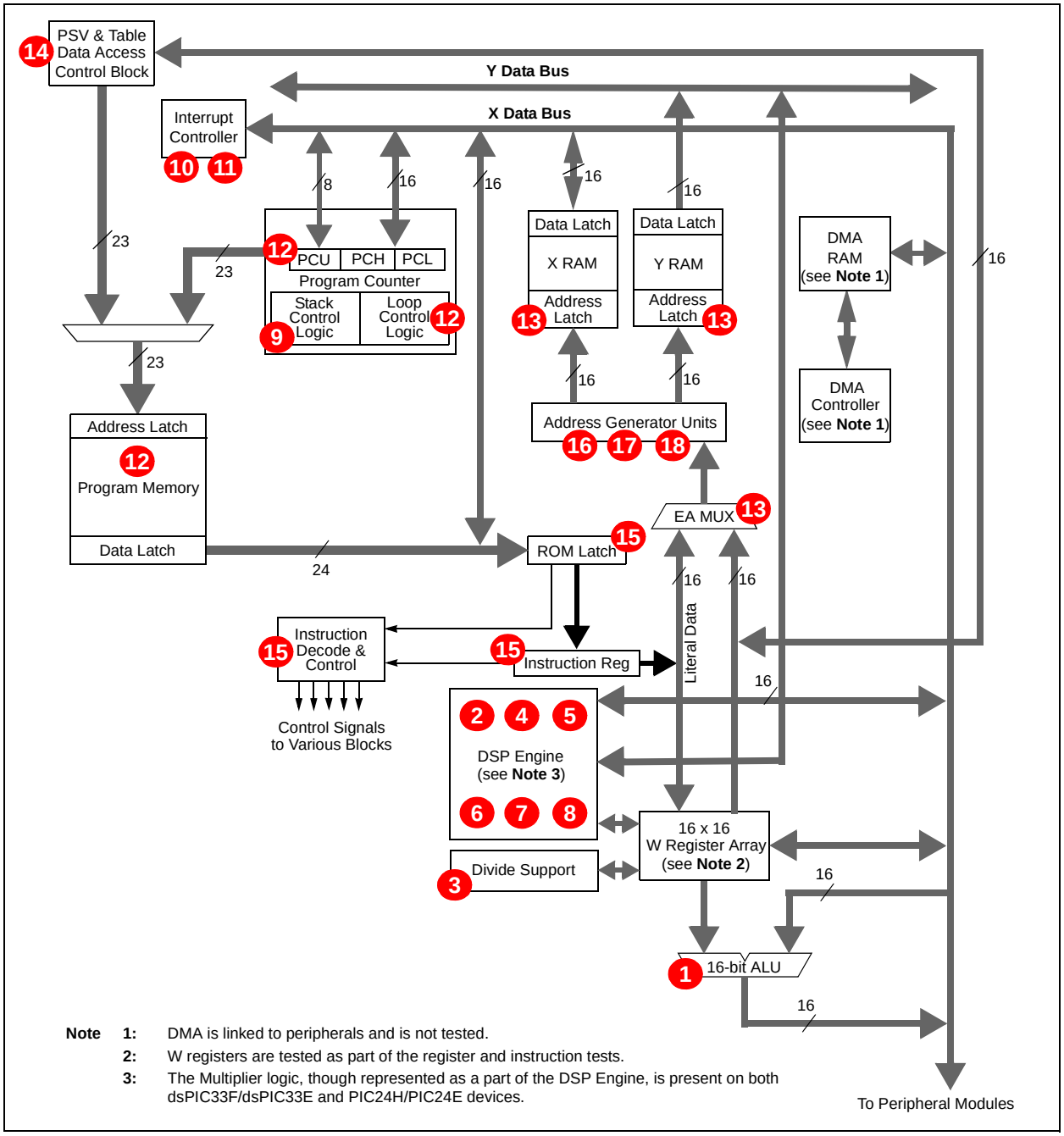
The entire set of CPU hardware modules were listed in the matrix and counted. Then, the hardware units tested by at least one test subset were counted based on code inspection. The percentage test coverage is then given by:

[(*Tested CPU Hardware Modules* / *Available CPU Hardware Modules*)] * 100.

The test coverage for bus structures is 100% ([(17/17)*100]).

Figure 4-1 and Figure 4-2 provide CPU block diagrams from the *"dsPIC33FJXXXGPX06/X08/X10 Data Sheet"* (DS70286) and the *"PIC24HJXXXGPX06/X08/X10 Data Sheet"* (DS70175), with labels correlating to the item numbers listed in Table 4-5.

FIGURE 4-1: dsPIC33FJXXXGPX06/X08/X10 CPU CORE BLOCK DIAGRAM

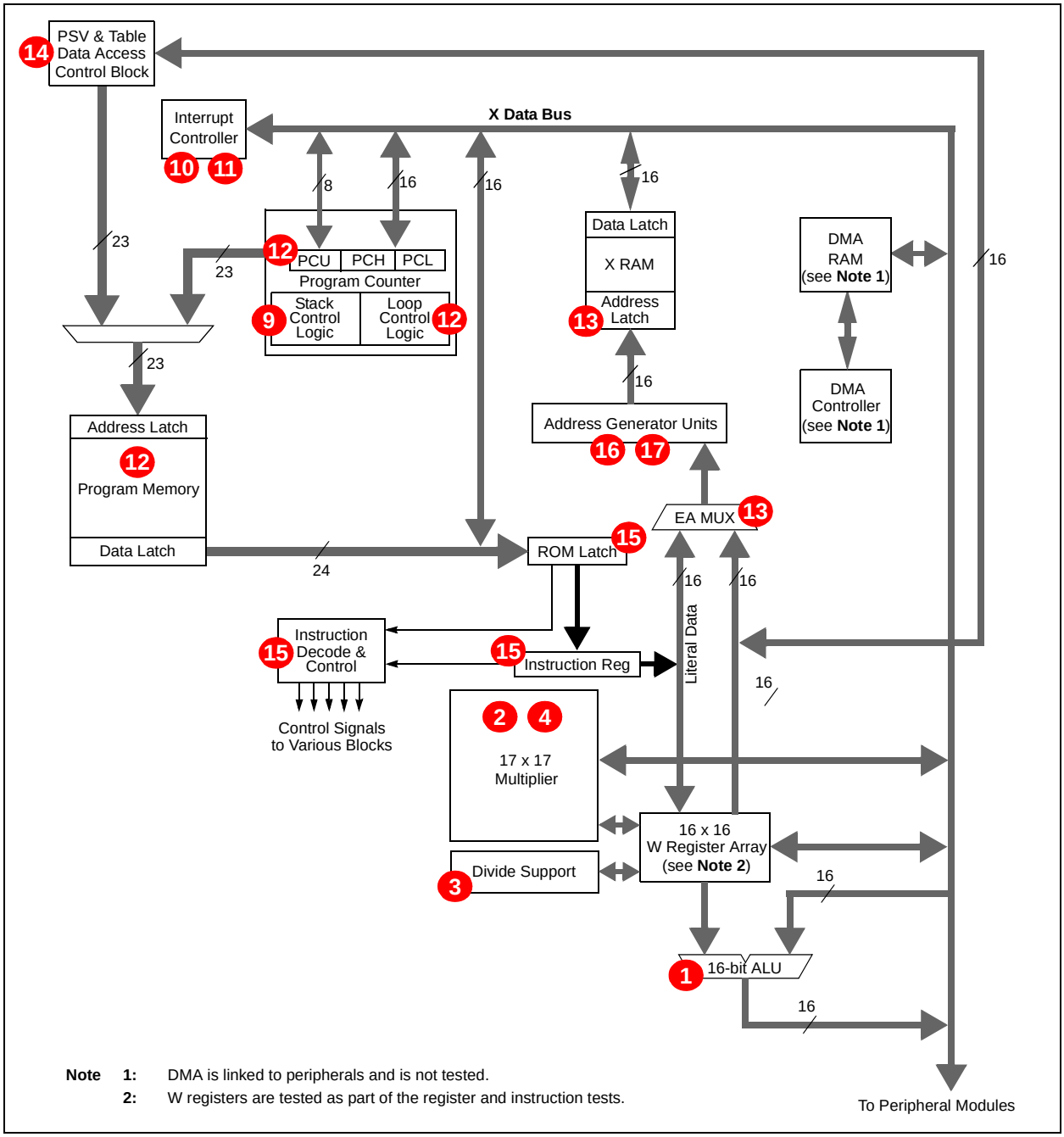


Note 1: DMA is linked to peripherals and is not tested.

2: W registers are tested as part of the register and instruction tests.

3: The Multiplier logic, though represented as a part of the DSP Engine, is present on both dsPIC33F/dsPIC33E and PIC24H/PIC24E devices.

FIGURE 4-2: PIC24HJXXXGPX06/X08/X10 CPU CORE BLOCK DIAGRAM



Note 1: DMA is linked to peripherals and is not tested.

2: W registers are tested as part of the register and instruction tests.

NOTES:

NOTES:

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Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
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India - Pune
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Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471- 6166
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Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
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Philippines - Manila
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Fax: 63-2-634-9069

Singapore
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Taiwan - Hsin Chu
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Fax: 886-3-5770-955

Taiwan - Kaohsiung
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