LAN9253

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN9253 2/3-Port EtherCAT® Device controller, which is the third port for flexible network configurations. LAN9253 supports 8/16-bit host bus, GPIO, SPI, and MII interface. The device can be configured as a three-port device, providing an additional MII port. This port can be connected to an external PHY, forming a tap along the current daisy chain or to another LAN9253, creating a four-port solution. The MII port can point upstream (as Port 0) or downstream (as Port 2). A summary of these items is provided in Section 14.0, "Hardware Checklist Summary," on page 37. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The LAN9253 implementor should have the following documents on hand:

- *LAN9253 Data Sheet*
- *LAN9253 Reference Design* (Note that Microchip Reference Designs are schematics only; there are no associated PCBs.)
- *EVB-LAN9253-SAMD51Customer Evaluation Board and Schematics*
- *EVB-LAN9253-ADD-ON-RevA Customer Evaluation Board and Schematics*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.
- Refer to Table 2-1 to check the LAN9253 QFN shape in your schematic.

TABLE 2-1: LAN9253 PINOUT

Pin Number	Pin Name	Pin Number	Pin Name
1	OSCI	34	SYNC0/LATCH0/PME
2	OSCO	35	D3/AD3/WD_TRIG/SIO3/EE_EMUL_SPI1
3	OSCVDD12	36	D6/AD6/DIGIO0/GPI0/GPO0/MII_RXCLK
4	OSCVSS	37	VDDIO
5	VDD33	38	VDDCR
6	VDDCR	39	D7/AD7/DIGIO1/GPI1/GPO1/MII_MDC
7	REG_EN	40	D8/AD8/DIGIO2/GPI2/GPO2/MII_MDIO
8	CLK_25/CLK_25_EN/XTAL_MODE	41	TESTMODE
9	ERRLED/PME/100FD_B/LEDPOL4	42	EESDA/TMS/EE_EMUL1
10	WAIT_ACK/PME/LATCH0/EE_EMUL_SPI3	43	EESCL/TCK/EE_EMUL2
11	RST#	44	IRQ/LATCH1
12	D2/AD2/SOF/SIO2/EE_EMUL_SPI0	45	RUNLED/STATE_RUNLED/E2PSIZE/EE_EMUL0/LEDPOL3
13	D1/AD1/EOF/SO/SIO1	46	LINKACTLED1/TDI/CHIP_MODE1/LEDPOL1
14	VDDIO	47	VDDIO
15	D14/AD14/DIGIO8/GPI8/GPO8/MII_TXD3/TX_SHIFT1	48	LINKACTLED0/TDO/CHIP_MODE0/100FD_A/LEDPOL0
16	D13/AD13/DIGIO7/GPI7/GPO7/MII_TXD2/TX_SHIFT0	49	D4/AD4/DIGIO3/GPI3/GPO3/MII_LINK
17	D0/AD0/WD_STATE/SI/SIO0	50	D5/AD5/OUTVALID/SCS#
18	SYNC1/LATCH1/PME	51	VDD33TXRX1
19	D9/AD9/LATCH_IN/SCK	52	TXNA
20	VDDIO	53	TXPA
21	D12/AD12/DIGIO6/GPI6/GPO6/MII_TXD1/100FD_B	54	RXNA
22	D11/AD11/DIGIO5/GPI5/GPO5/MII_TXD0/100FD_A	55	RXPA
23	D10/AD10/DIGIO4/GPI4/GPO4/MII_TXEN	56	VDD12TX1
24	VDDCR	57	RBIAS
25	A1/ALELO/OE_EXT/MII_CLK25/EE_EMUL_SPI2	58	VDD33BIAS
26	A3/BE0/DIGIO11/GPI11/GPO11/MII_RXDV	59	VDD12TX2
27	A4/BE1/DIGIO12/GPI12/GPO12/MII_RXD0	60	RXPB
28	CS/DIGIO13/GPI13/GPO13/MII_RXD1	61	RXNB
29	A2/ALEHI/DIGIO10/GPI10/GPO10/LINKACTLED2/EE_EMUL_ALELO_POL/MII_LINKPOL/LEDPOL2	62	TXPB
30	WR/ENB/DIGIO14/GPI14/GPO14/MII_RXD2	63	TXNB
31	RD/RD_WR/DIGIO15/GPI15/GPO15/MII_RXD3	64	VDD33TXRX2
32	VDDIO	65	EDP Ground, Exposed Die Paddle Ground, Pad on Bottom of Package
33	A0/D15/AD15/DIGIO9/GPI9/GPO9/MII_RXER		

3.0 POWER

3.1 +3.3V Power Supply Connections

- The supply for the two internal regulators on the LAN9253 QFN is pin 5 (**VDD33**). This pin requires a connection to +3.3V. The **VDD33** power pin should have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

Note: +3.3V must be supplied to this pin even if the internal regulators are disabled.

- The analog supply (**VDD33TXRX1**) pin on the LAN9253 QFN is pin 51. It requires a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33TXRX1** pin should have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.
- The analog supply (**VDD33TXRX2**) pin on the LAN9253 QFN is pin 64. It requires a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33TXRX2** pin should have 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.
- The **VDD33BIAS** (pin 58) pin serves as the Host bias voltage supply for the LAN9253. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. The **VDD33BIAS** pin should have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

3.2 +1.8V to +3.3V Variable I/O Power Supply Connections

- The variable I/O supply (**VDDIO**) pins on the LAN9253 QFN are 14, 20, 32, 37, and 47. They require an externally supplied voltage supply between +1.8V and +3.3V.
- Each **VDDVARIO** pin should have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

3.3 VDDCR

3.3.1 INTERNAL REGULATOR ENABLE MODE (REG_EN PIN PULL-UP)

- The **VDDCR** (pins 6, 24, and 38) pins are used to provide bypassing for the +1.2V core regulator. Pins 24 and 38 require two 0.1 µF (or smaller) decoupling capacitors. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 6 requires a bulk capacitor placed as close as possible to pin 6. The bulk capacitor must have a value of at least 1.0 µF and must have an equivalent series resistance (ESR) of 1.0 µF. Microchip recommends a very low 0.1Ω ESR ceramic capacitor for design stability. In addition, pin 6 also requires a 470 pF bypass capacitor. Other values, tolerances, and characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only. Do not power other external circuits or devices with this supply.

- **OSCVDD12** (pin 3) can be floating in the internal regulator Enable mode.
- The **VDD12TX1** (pin 56) and **VDD12TX2** (pin 59) pins supply power from **VDDCR** pin through a ferrite bead for the two Ethernet blocks. These two pins must be tied together. These two pins must be connected to **VDDCR** through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VDD12TX1** and **VDD12TX2** pins should each have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

3.3.2 INTERNAL REGULATOR DISABLE MODE (REG_EN PIN PULL-DOWN)

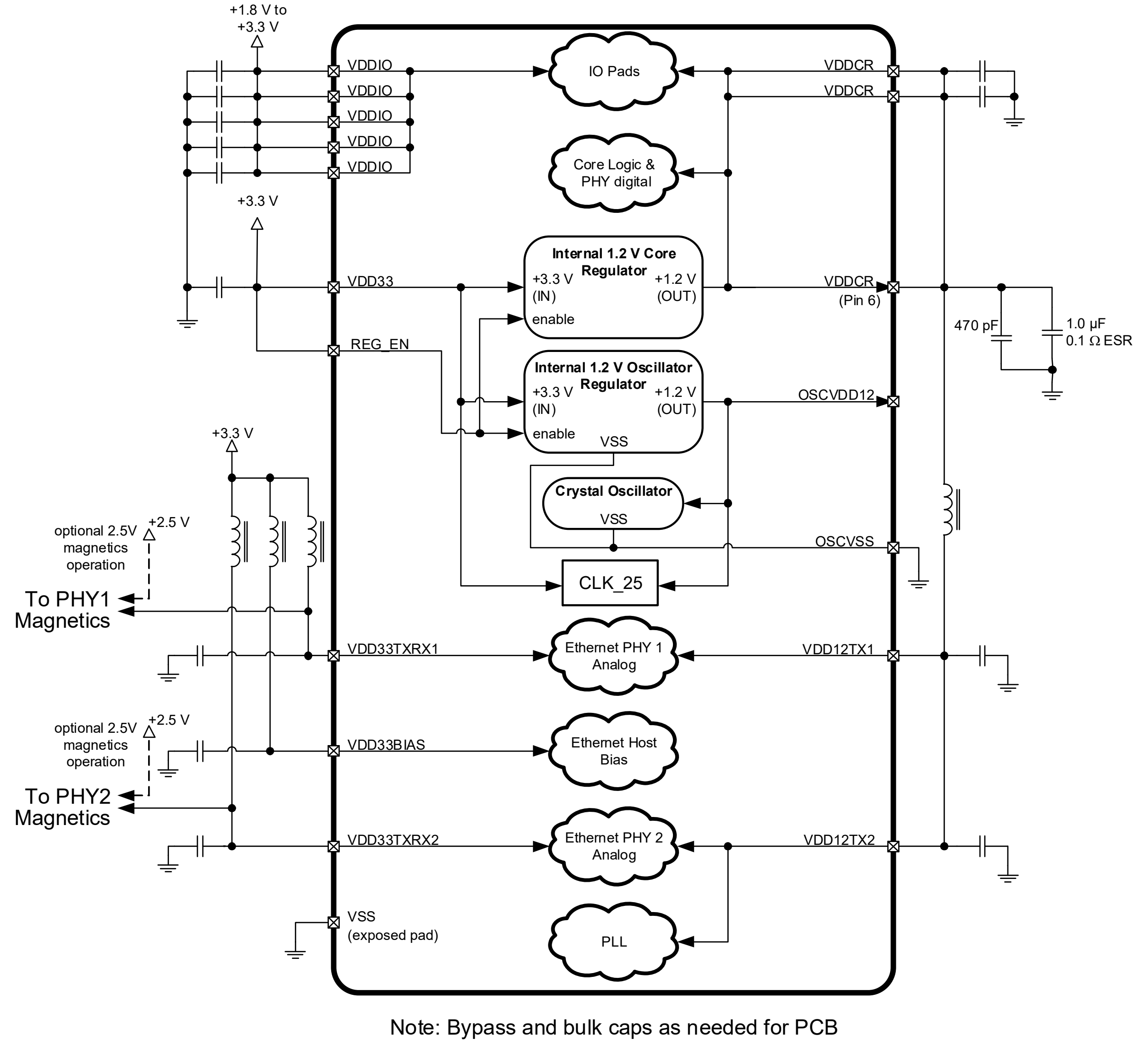
- The **VDDCR** (pins 6, 24, and 38) pins are used to provide bypassing for the +1.2V core regulator. All **VDDCR** pins require three 0.1 µF (or smaller) decoupling capacitors. Each capacitor should be located as close as possible to its pin without using vias.
- **OSCVDD12** (pin 3) also needs a 0.1 µF (or smaller) decoupling capacitors in the internal regulator Disable mode.
- **VDD12TX1** (pin 56) and **VDD12TX2** (pin 59) supply power from **VDDCR** through a ferrite bead for the two Ethernet blocks. These two pins must be tied together. These two pins must be connected to **VDDCR** through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VDD12TX1** and **VDD12TX2** pins should each have one 0.1 µF (or smaller) capacitor to decouple the LAN9253. The capacitor size should be SMD_0603 or smaller.

Caution: If internal 1.2V regulators are disabled, use an external 1.2V power supply connected to VDDCR pins, OSCVDD12 pin, and through a ferrite bead to VDD12TX1 and VDD12TX2 pins.

3.4 Power and Ground Connections

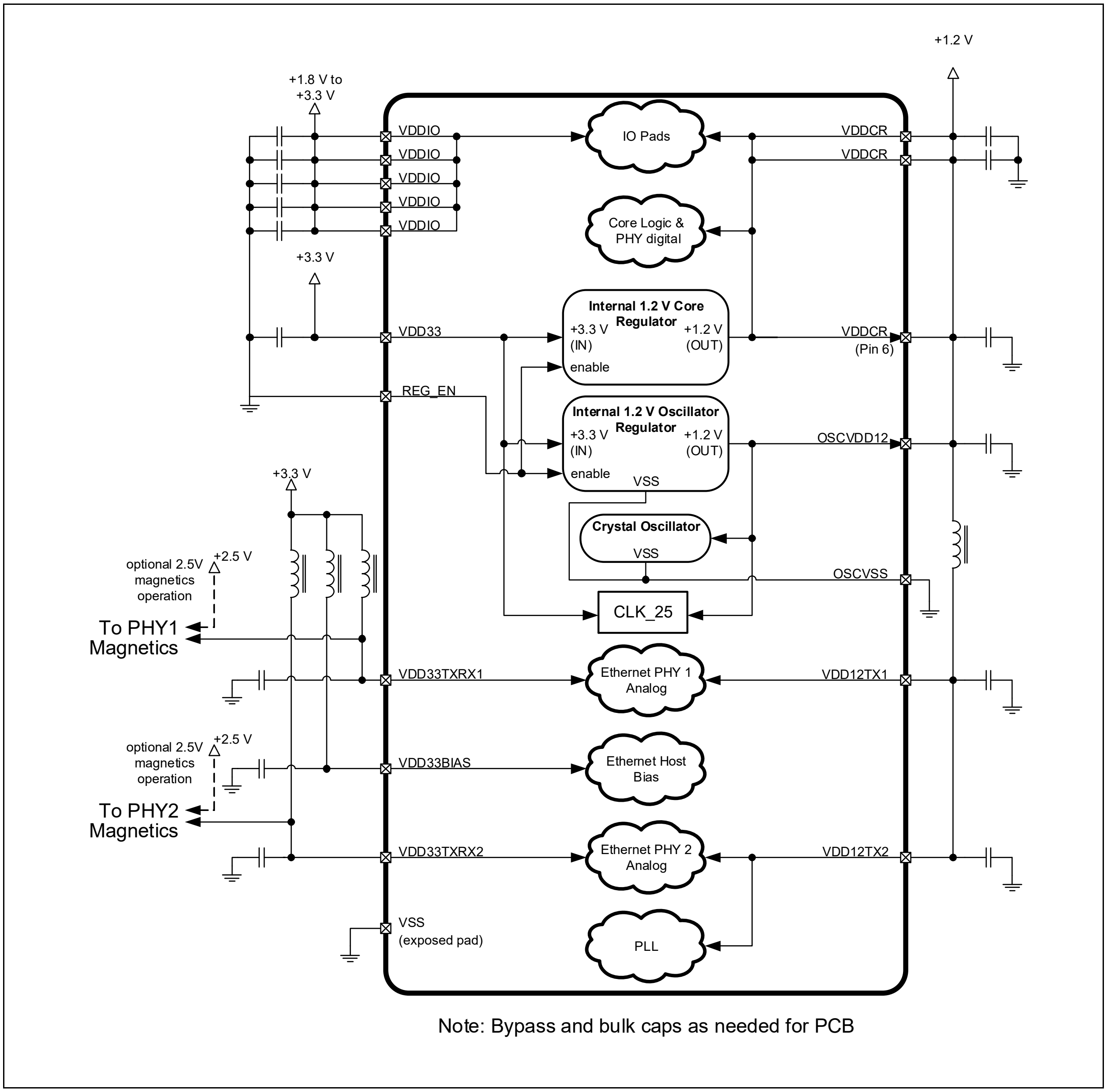
- All grounds, the digital ground pins (**GND**), the core ground pins (**GND_CORE**), and the analog ground pins (**VSS_A**) on the LAN9253 QFN, are all connected internally to the exposed die paddle ground (**VSS**) as system ground. The EDP ground pad on the underside of the LAN9253 must be connected directly to a solid, contiguous ground plane.
- On the PCB, one system ground is recommended. Running separate digital ground and analog ground planes for any of Microchip's LAN products is not recommended.
- For the power connection with the regulators enabled and the regulator disabled, see Figure 3-1 and Figure 3-2.

FIGURE 3-1: POWER CONNECTION WITH REGULATORS ENABLED (REG_EN PIN PULL-UP)



Note: Bypass and bulk caps as needed for PCB

FIGURE 3-2: POWER CONNECTION WITH REGULATORS DISABLED (REG_EN PIN PULL-DOWN)



- The **OSCVDD12** (pin 3) pin is supplied by one of the internal +1.2V regulators of the LAN9253 and can be left as a no-connection in this mode (REGEN = high). When REGEN = low, this pin must be supplied by an external +1.2V power supply, and then add a 0.1 µF (or smaller) decoupling capacitor.
- The **OSCVSS** (pin 4) pin should be connected directly to system ground for all applications.
- In addition to having decouple capacitors for all power pins, be sure to incorporate enough bulk capacitors (4.7-22 µF caps) for each power plane.

3.5 Placing Power Pins in PCB Layout

3.5.1 +3.3V POWER SUPPLY CONNECTIONS

- Place one of each of the following decoupling capacitors for the LAN9253 QFN as close to the power pin as possible:
  - VDD3
  - VDD33TXRX1
  - VDD33TXRX2
  - VDD33BIAS
- Use an SMD_0603 package to make each task easier.

3.5.2 +1.8V TO +3.3V VARIABLE I/O POWER SUPPLY CONNECTIONS

- Place the five VDDIO decoupling capacitors for the LAN9253 QFN as close to each power pin as possible. Use an SMD_0603 package to make this task easier.

3.5.3 VDDCR

- For **VDDCR** (pins 6, 24, and 38), place all decoupling capacitors as close to each **VDDCR** pin as possible (refer to Figure 3-1 and Figure 3-2).
- Each of the **VDD12TX1** (pin 56) and **VDD12TX2** (pin 59) pins requires a 0.1 µF (or smaller) bypass capacitor placed as close as possible to both pins.

3.5.4 GROUND CONNECTIONS

- If using the magnetics and RJ45 connector, a chassis ground should be used for the line side of the magnetics and the metal case of the RJ45 connector. The system ground and the chassis ground should be tied together by a component (ferrite bead, resistor or capacitor). Leave the component out, and the two grounds are separate. Short them together with a zero ohm resistor or short them together with a ferrite bead or a capacitor for best performance. An SMD_0805 or 1210 footprint can be used for the component (ferrite bead, resistor or capacitor).

3.6 Routing Power Pins in PCB Layout

3.6.1 +3.3V POWER SUPPLY CONNECTIONS

- Route the **VDD33** pin of the LAN9253 QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33 decoupling capacitor for the LAN9253 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the **VDD33TXRX1** pin of the LAN9253 QFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33TXRX1 decoupling capacitor for the LAN9253 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the VDD33TXRX1 bulk capacitor for the LAN9253 QFN power pins as short as possible directly to the VDD33TXRX1 power plane.
- Route the **VDD33TXRX2** pin of the LAN9253 QFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.
- Route the VDD33TXRX2 decoupling capacitor for the LAN9253 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the VDD33TXRX2 bulk capacitor for the LAN9253 QFN power pin as short as possible directly to the VDD33TXRX2 power plane.
- Route the **VDD33BIAS** (pin 58) of the LAN9253 QFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short and wide as possible.

- Route the VDD33BIAS decoupling capacitor for the LAN9253 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V and system ground plane) for the capacitor.
- Route the VDD33BIAS bulk capacitor for the LAN9253 QFN power pin as short as possible directly to the VDD33BIAS power plane.
- Place one VDD33TXRX2 decoupling capacitor for the LAN9253 QFN as close to the power pin as possible. Using an SMD_0603 package makes this task easier.

3.6.2 +1.8V TO +3.3V VARIABLE I/O POWER SUPPLY CONNECTIONS

- Route the five **VDDIO** pins of the LAN9253 QFN directly into a solid, +1.8V to +3.3V power plane. The pin-to-plane trace should be as short and wide as possible.
- Route the five VDDIO decoupling capacitors for the LAN9253 QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+V power plane and system ground plane) for each capacitor.

3.6.3 VDDCR

- The **VDDCR** (pins 6, 24, and 38) pins must be routed with a heavy, wide trace with multiple vias to the three decoupling capacitors and the single bulk capacitor associated with it. All three pins and the capacitors should be routed directly into a solid, +1.2V power plane. The pin-to-plane trace should be as short and wide as possible.
- The **VDD12TX1** (pin 56) and **VDD12TX2** (pin 59) pins must be routed with a heavy, wide trace with multiple vias to the two decoupling capacitors and the single bulk capacitor associated with them. Pins 56 and 59 and the capacitors should be routed through the associated ferrite bead directly into a solid, +1.2V power plane (VDDCR).

3.6.4 GROUND CONNECTIONS

- The single ground pin (pin 65, EDP) on the LAN9253 QFN should be connected directly into a solid, contiguous, system ground plane. The EDP pad on the component side of the PCB should be connected to the internal system ground plane with 36 power vias in a 6x6 grid.
- It is recommended that all ground pins be tied together to the same ground plane. Running separate ground planes for any of Microchip’s LAN products is not recommended.

4.0 ETHERNET/ETHERCAT® SIGNALS

The LAN9253 has two integrated 100 Mbps Ethernet transceivers that are compliant with IEEE 802.3/802.3u standard to be compatible with EtherCAT P.

4.1 LAN9253 Copper Port A Differential Pair PHY Interface

- The **TXPA** (pin 53) pin is the transmit (TX) differential pair output positive connection from the primary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX1** (created from +3.3V). This pin also connects to the TX channel of the primary magnetics.
- The **TXNA** (pin 52) pin is the TX differential pair output negative connection from the primary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX1** (created from +3.3V). This pin also connects to the TX channel of the primary magnetics.
- For Port A TX channel connection and termination details, refer to Figure 4-1 and Figure 4-2.
- The **RXPA** (pin 55) pin is the receive (RX) differential pair input positive connection to the primary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX1** (created from +3.3V). This pin also connects to the RX channel of the primary magnetics.
- The **RXNA** (pin 54) pin is the RX differential pair input negative connection to the primary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX1** (created from +3.3V). This pin also connects to the RX channel of the primary magnetics.
- For Port A RX channel connection and termination details, refer to Figure 4-1 and Figure 4-2.
- For added EMC flexibility in a LAN9253 design, the designer should include four low-valued capacitors on the **TXPA**, **TXNA**, **RXPA**, and **RXNA** pins. Low-valued capacitors (less than 22 pF) can be added to each line and terminated to system ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

4.2 LAN9253 Copper Port B Differential Pair PHY Interface

- The **TXPB** (pin 62) pin is the TX differential pair output positive connection from the secondary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX2** (created from +3.3V). This pin also connects to the TX channel of the secondary magnetics.
- The **TXNB** (pin 63) pin is the TX differential pair output negative connection from the secondary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX2** (created from +3.3V). This pin also connects to the TX channel of the secondary magnetics.
- For Port B TX channel connection and termination details, refer to Figure 4-1 and Figure 4-2.
- The **RXPB** (pin 60) pin is the RX differential pair input positive connection to the secondary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX2** (created from +3.3V). This pin also connects to the RX channel of the secondary magnetics.
- The **RXNB** (pin 61) pin is the RX differential pair input negative connection to the primary internal PHY. It requires a 49.9Ω, 1.0% pull-up resistor to **VDD33TXRX2** (created from +3.3V). This pin also connects to the RX channel of the secondary magnetics.
- For Port B RX channel connection and termination details, refer to Figure 4-1 and Figure 4-2.
- For added EMC flexibility in a LAN9253 design, the designer should include four low-valued capacitors on the **TXPB**, **TXNB**, **RXPB**, and **RXNB** pins. Low-valued capacitors (less than 22 pF) can be added to each line and terminated to system ground. These components can be added to the schematic and should be designated as DNP.

FIGURE 4-1: TRANSMIT CHANNEL CONNECTIONS AND TERMINATIONS

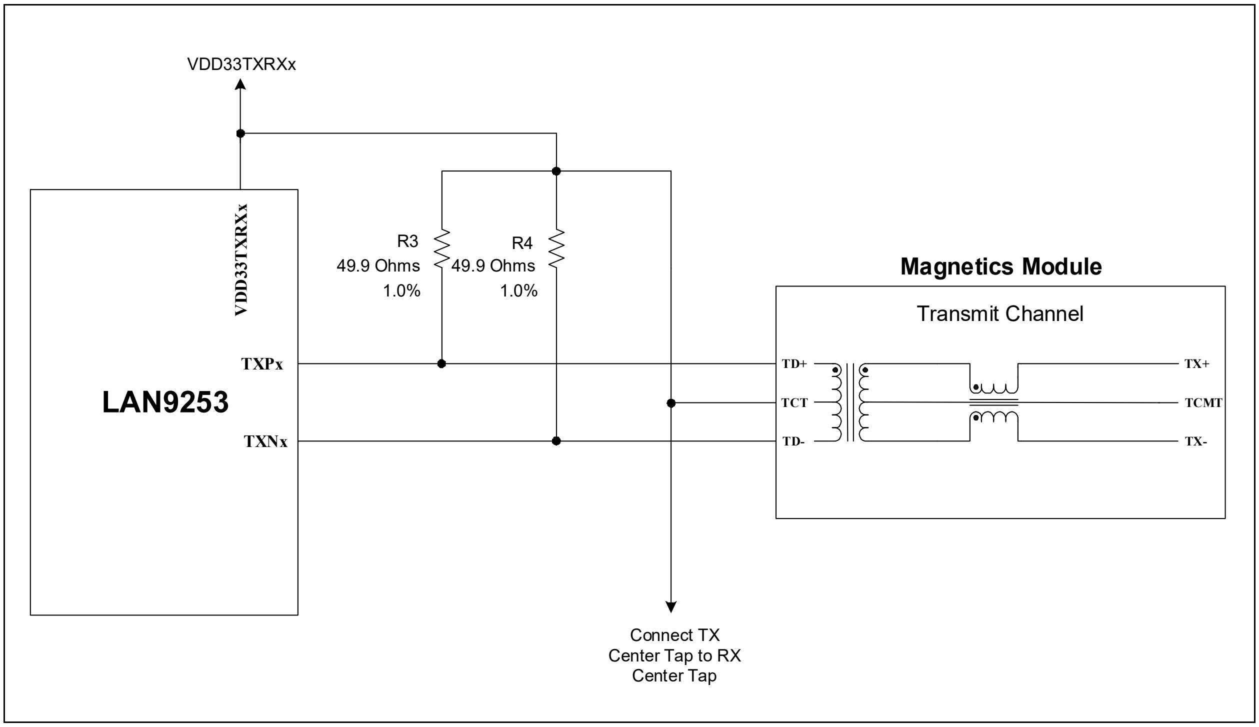
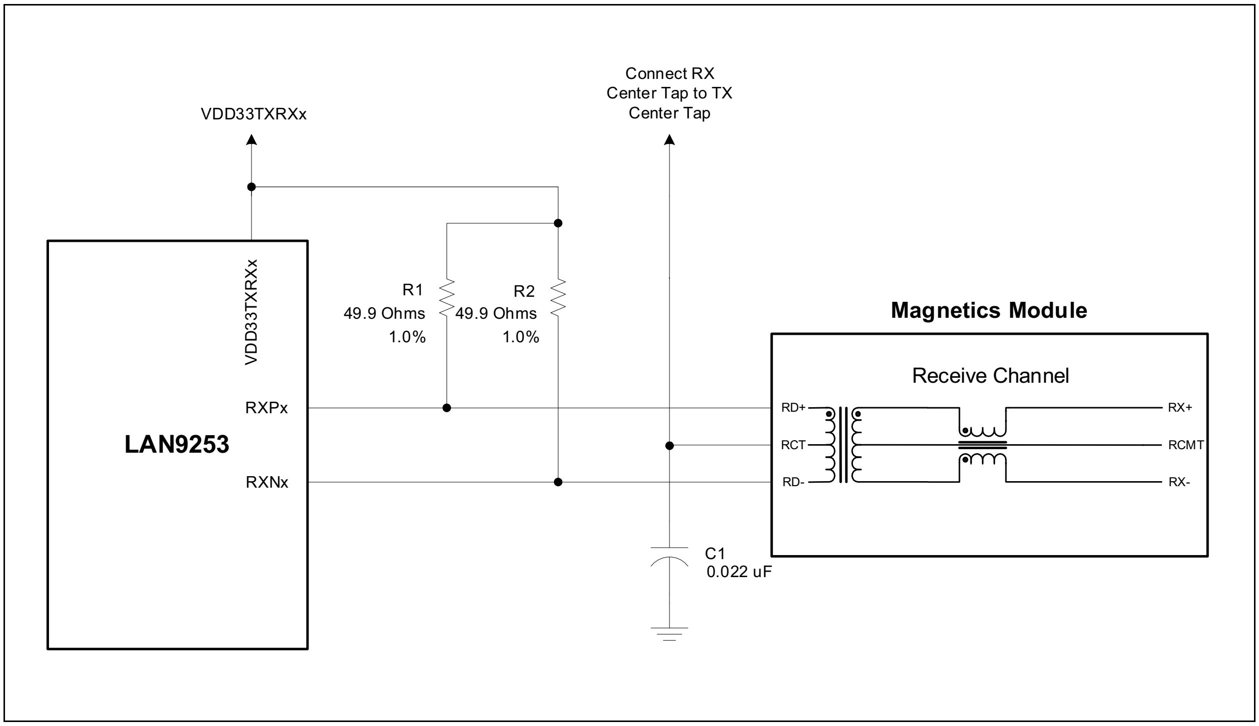


FIGURE 4-2: RECEIVE CHANNEL CONNECTIONS AND TERMINATIONS



4.3 LAN9253 Copper Port A Differential Pair PHY Magnetics

- The center tap connection on the LAN9253 side for the TX channel must be connected to **VDD33TXRX1** (created from +3.3V) directly. The TX channel center tap of the magnetics also connects to the RX channel center tap of the magnetics.
- The center tap connection on the LAN9253 side for the RX channel is connected to the TX channel center tap on the primary magnetics. In addition, a 0.022 µF capacitor is required from the RX channel center tap of the primary magnetics to system ground.
- The center tap connection on the cable side (RJ45 side) for the primary TX channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground.
- Only one 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC):
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to **TXPA** (pin 53) of the LAN9253 QFN.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to **TXNA** (pin 52) of the LAN9253 QFN.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to **RXPA** (pin 55) of the LAN9253 QFN.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to **RXNA** (pin 54) of the LAN9253 QFN.

4.4 LAN9253 Copper Port B Differential Pair PHY Magnetics

- The center tap connection on the LAN9253 side for the TX channel must be connected to **VDD33TXRX2** (created from +3.3V) directly. The TX channel center tap of the magnetics also connects to the RX channel center tap of the magnetics.
- The center tap connection on the LAN9253 side for the RX channel is connected to the TX channel center tap on the primary magnetics. In addition, a 0.022 µF capacitor is required from the RX channel center tap of the primary magnetics to system ground.
- The center tap connection on the cable side (RJ45 side) for the primary TX channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the primary RX channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground.
- Only one 1000 pF, 2 kV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC):
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to **TXPB** (pin 62) of the LAN9253 QFN.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to **TXNB** (pin 63) of the LAN9253 QFN.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to **RXPB** (pin 60) of the LAN9253 QFN.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to **RXNB** (pin 61) of the LAN9253 QFN.
- When using the LAN9253 in the HP Auto-MDIX mode of operation, the use of an Auto-MDIX style magnetics module should be required.

4.5 LAN9253 Port A and Port B Differential Pair Between Magnetics and RJ45

- Pins 4 and 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor (C_{rjterm}). There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor (C_{rjterm}).
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

- Pins 7 and 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor (C_{rjterm}). There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor (C_{rjterm}).
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
- The RJ45 shield should be attached directly to chassis ground.

4.6 Using RJ45 with Integrated LED

- The user can utilize the RJ45 connector with integrated LED components if the product working environment is not very noisy.
- If the designed product operates in an electrically noisy outside environment, using RJ45 with integrated LED is not recommended. This is because the outside interference signal or voltage could be coupled to the LED circuit through the line side of RJ45 due to the LED circuit directly connected to chip and system power or ground. It is better to use independent LED components.
- If the user needs to utilize the RJ45 with an integrated LED circuit in a noisy environment, consider adding TVS diodes to protect the chip.

4.7 Placing Copper Ports in PCB Layout

4.7.1 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS INTERFACE

- If the Auto-MDIX functionality is enabled, place the 49.9Ω TX termination pull-up (**TXPA** and **TXPB** pins) as close to the LAN9253 as possible. If the Auto-MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
- If the Auto-MDIX functionality is enabled, place the 49.9Ω TX termination pull-up (**TXNA** and **TXNB** pins) as close to the LAN9253 as possible. If the Auto-MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
- Place the 49.9Ω RX termination pull-up (**RXPA** and **RXPB** pins) as close to the LAN9253 as possible.
- Place the 49.9Ω RX termination pull-up (**RXNA** and **RXNB** pins) as close to the LAN9253 as possible.
- Place the four optional, low-valued, common-mode capacitors for each differential signal as close as possible to the magnetics. They should be placed as to create the smallest possible stub.

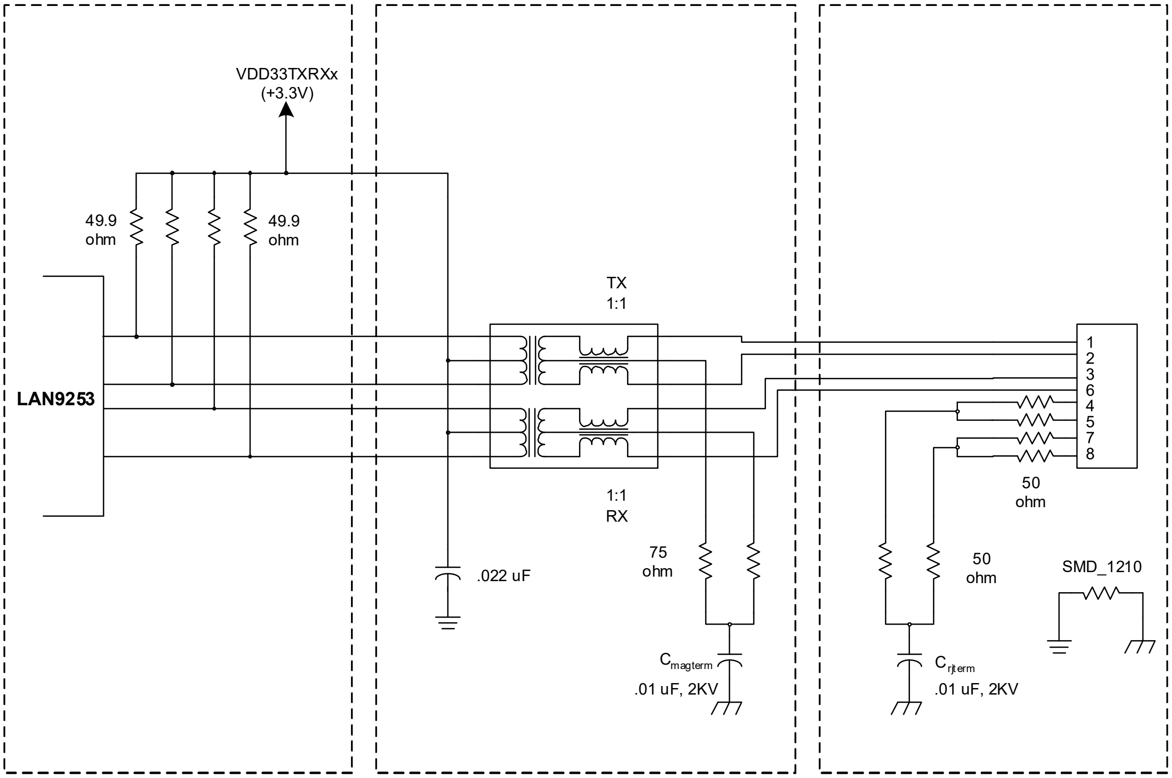
4.7.2 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS

- Place the 0.022 µF TX/RX channel center tap termination capacitor as close to the magnetics as possible.
- Place the 75Ω cable side center tap termination resistors and the 1000 pF, 2 kV capacitor ($C_{magterm}$) as close to the magnetics as possible.

4.7.3 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS TO RJ45 CONNECTORS

- Place the RJ45 connector, the magnetics, and the LAN9253 QFN as close together as possible. If this is not possible, keep the RJ45 connector and the magnetics as close as possible.
- Select and place the magnetics as to set up the best routing scheme from the LAN9253 QFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pinouts to facilitate this operation. Investigate Tab-Up and Tab-Down RJ45 connectors in order to facilitate layout.
- Place the unused wire pair termination resistors and the 1000 pF, 2 kV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.
- Make sure to not place any other components in or near the TX channel and RX channel lanes of the PCB. These lanes should be clear of any other signals and components.
- For the copper ports from LAN9253 through the magnetics to RJ45 connector placement, refer to Figure 4-3.

FIGURE 4-3: COMPONENTS PLACEMENT FOR COPPER PORTS



Locate the four 49.9 ohm differential terminations close to the LAN9253

Locate these three resistors and two caps close to the magnetics

Locate all these components close to the RJ45 connector

4.8 Routing Copper Ports in PCB Layout

4.8.1 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS INTERFACE

- The traces connecting the TX outputs (**TXPA** and **TXNA** pins, or **TXPB** and **TXNB** pins) to the magnetics must be run as differential pairs. The differential impedance should be 100Ω.
- The traces connecting the RX inputs (**RXPA** and **RXNA** pins, or **RXPB** and **RXNB** pins) from the magnetics must be run as differential pairs. The differential impedance should be 100Ω.
- For differential traces running from the LAN PHY to the magnetics, Microchip recommends routing these traces on the component side of the PCB with a contiguous system ground plane on the next layer. This minimizes the use of vias and avoids impedance mismatches by switching PCB layers.
- The VDD33TXRX1 of Port A and the VDD33TXRX2 of Port B power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

4.8.2 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS

- The traces connecting the TX outputs from the magnetics to pins 1 and 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100Ω.
- The traces connecting the RX inputs on the magnetics from pins 3 and 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100Ω.
- For differential traces running from the magnetics to the RJ45 connector, Microchip recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This minimizes the use of vias and minimizes any unwanted noise from coupling into the differential pairs. The plane clear-out boundary is usually halfway through the magnetics.

4.8.3 COPPER PORT A AND PORT B DIFFERENTIAL PAIRS THROUGH MAGNETICS TO RJ45 CONNECTORS

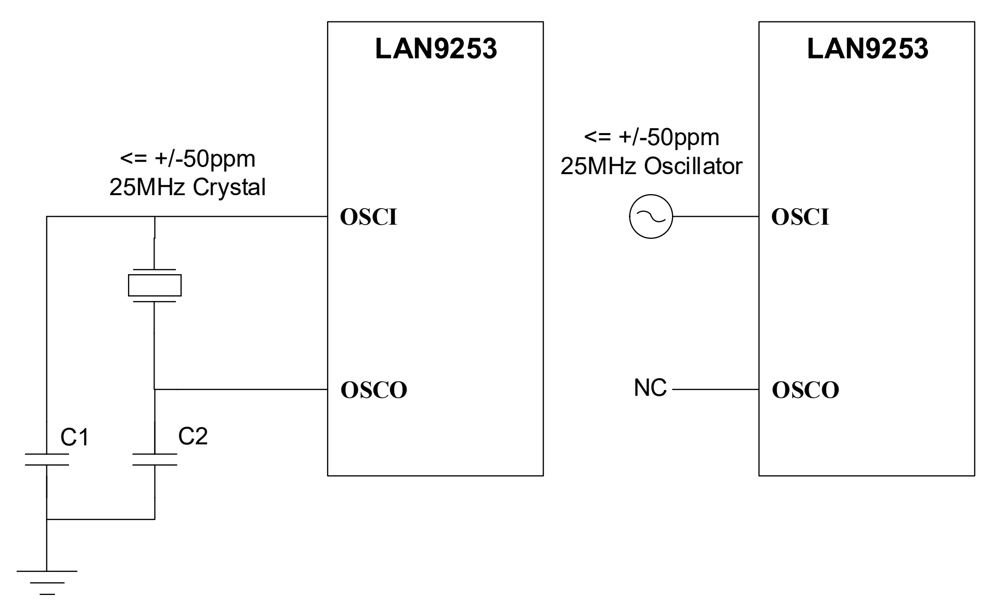
- Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and may cause EMC problems.
- Construction of a separate chassis ground that can be easily connected to system ground at one point is also recommended. This plane provides the lowest impedance path to earth ground.

5.0 CLOCK CIRCUIT

5.1 Crystal or Oscillator Clock Connections

- A 25.000 MHz crystal must be used with the LAN9253 QFN. For exact specifications and tolerances refer to the latest revision *LAN9253 Data Sheet*.
- The **OSCI** (pin 1) pin on the LAN9253 QFN is the clock circuit input. This pin requires a 27-33 pF capacitor to system ground. One side of the crystal connects to this pin.
- The **OSCO** (pin 2) pin on the LAN9253 QFN is the clock circuit output. This pin requires a matching 27-33 pF capacitor to ground and the other side of the crystal.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L specification of the crystal and the stray capacitance value. Refer to the crystal data sheet for C_L required. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- For proper operation, the additional external 1.0 MΩ resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN9253 QFN.
- Alternately, a 25.000 MHz clock oscillator may be used to provide the clock source for the LAN9253. When using a single-ended clock source, **OSCI** (pin 1) connects to a 3.3V tolerant oscillator. **OSCO** (pin 2) should be left floating as No Connect (NC). See Figure 5-1.
- Select a minimum 50 uW (higher better), typical 300 uW drive-level crystal or oscillator.
- **Design Verification Tip:** Microchip recommends taking advantage of the Clock Output Test mode in the LAN9253. In order to facilitate system-level validation and debug, the crystal clock can be enabled onto the **IRQ** pin by setting the IRQ Clock Select (IRQ_CLK_SELECT) bit of the Interrupt Configuration Register (IRQ_CFG). The **IRQ** pin should be set to a push-pull driver by using the IRQ Buffer Type (IRQ_TYPE) bit for the best result. Be sure to include a test pin on the **IRQ** (pin 44) pin and a ground pin close to the test pin. Using a high-quality, precise frequency counter with 8-digits or better will accurately determine the frequency of the 25.000 MHz in the design. Adjusting the crystal circuit load caps slightly will fine tune the frequency of the circuit.

FIGURE 5-1: LAN9253 CRYSTAL OR OSCILLATOR CONNECTIONS



5.2 Other Clock Pins

- **CLK_25/CLK_25_EN/XTAL_MODE** (pin 8) is an additional 25 MHz clock output pin to provide 25 MHz crystal clock for an external device. Three cases are as follows:
  - If the 25 MHz clock output is not needed, connect pin 8 to ground directly to disable the 25 MHz clock output on pin 8 **CLK_25**.
  - If the 25MHz clock for external device is needed, a resistor voltage divider of two resistors can be used for 1.5V voltage level as **CLK_25_EN** to enable 25 MHz output from pin 8 **CLK_25**.
  - If two LAN9253 with 25 MHz clock are used in the clock daisy chaining configuration, using the **CLK_25** of the previous devices as the input clock source, pin 1 **OSCI** should be set to Schmitt trigger input mode via the pin 8 **XTAL_MODE** strap-in by a pull-up resistor to VDD33.

5.3 Placing and Routing Crystal in PCB Layout

- Place the 25.000 MHz crystal and the associated 15-33 pF capacitors as close together as possible and as close to the LAN9253 QFN (**OSCI** and **OSCO** pins) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, and so on.)
- Place all the crystal components on the component side of the PCB with a system ground plane layer on the next layer. This minimizes vias in the circuit connections and assures that all the crystal components are referenced to the same reference plane.
- The routing for the crystal or clock circuitry should be kept as small and short as possible.
- A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the system ground plane directly below it.

6.0 CONFIGURATION FOR SYSTEM APPLICATIONS

The LAN9253 applications can be divided into the following modes. Refer to Figure 6-11 for detail.

- Microcontroller Mode with Host Bus Interface
- Microcontroller Mode with SPI/SQI Interface
- Expansion Mode with MII to External PHY
- Digital I/O Mode

6.1 Microcontroller Mode with Host Bus Interface

- The integrated Host Bus Interface (HBI) supports 8/16-bit operation with big, little, and mixed endian operations. The MCU through the HBI to the EtherCAT Device controller facilitates the transfer of data information between the host MCU and the EtherCAT Device controller.

6.2 Microcontroller Mode with SPI/SQI Interface

- The device can be accessed via SPI/SQI with MCU, while also providing up to 16 inputs or outputs for general purpose usage. An SPI/SQI (Quad SPI) Client controller provides a low pin count synchronous device interface that facilitates communication between the device and a host system.
- The MCU through the SPI/SQI to the EtherCAT Device controller facilitates the transfer of the data information between the host MCU and the EtherCAT Device controller.

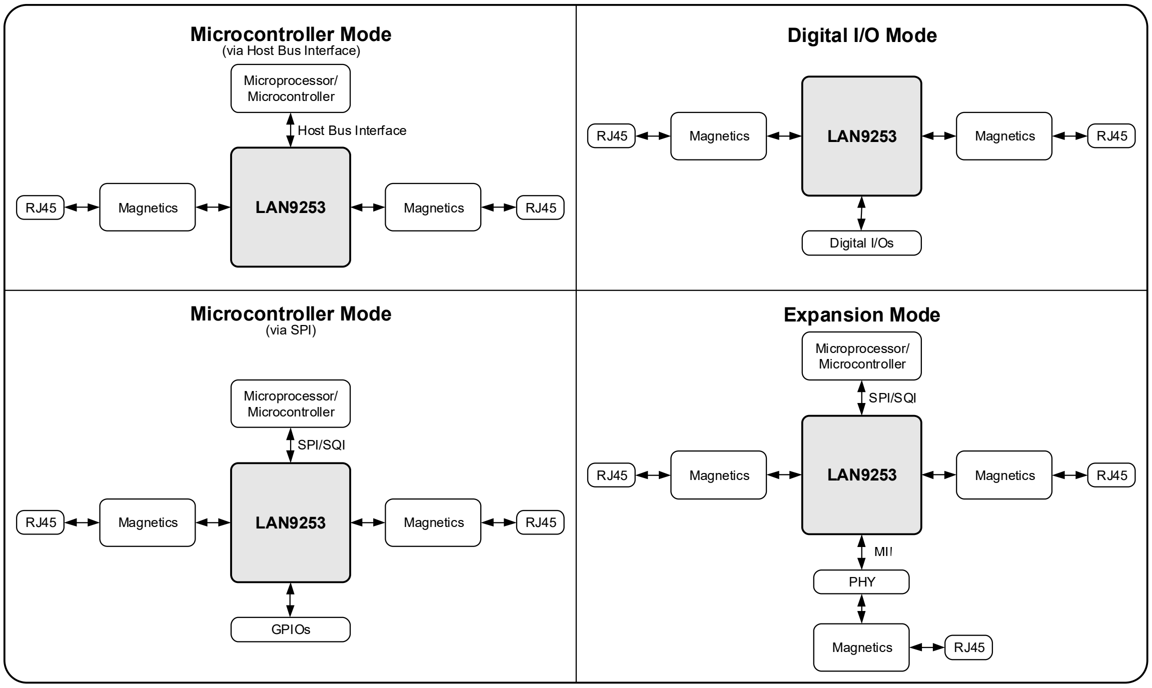
6.3 Expansion Mode with MII to External PHY

- While the device is in SPI/SQI mode, a third networking port can be enabled to provide an additional MII port. This port can be connected to an external PHY to enable star or tree network topologies, or to another LAN9253 to create a four-port solution. This port can be configured for upstream or downstream direction.

6.4 Digital I/O Mode

- For simple digital modules without MCU, the LAN9253 can operate in Digital I/O mode where 16 digital signals can be controlled or monitored by the EtherCAT host. Up to seven control signals are also provided.

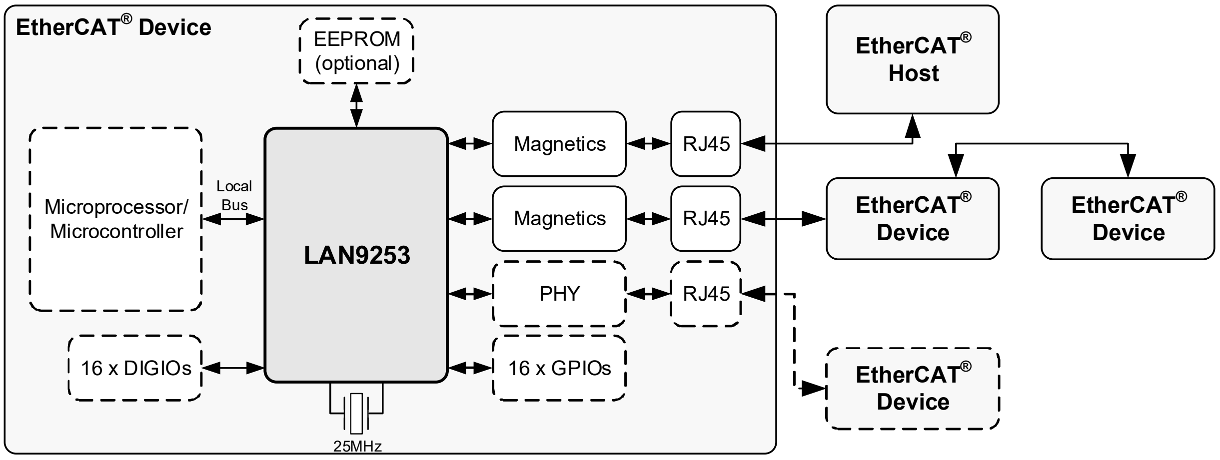
FIGURE 6-1: LAN9253 MODES OF OPERATION



6.5 System Block Diagram

- The complete system application block diagram is illustrated in Figure 6-2.
- Microprocessor/Microcontroller connects through local bus to LAN9253, DIGIO, and (optional) EEPROM.
- Port 0 (Port A) connects to EtherCAT Host controller in 3-Port Downstream mode.
- Port 1 (Port B) connects to EtherCAT Device controller in 3-Port Downstream mode.
- Port 2 MAC MII connects to an external PHY to another EtherCAT Device controller.

FIGURE 6-2: LAN9253 SYSTEM BLOCK DIAGRAM

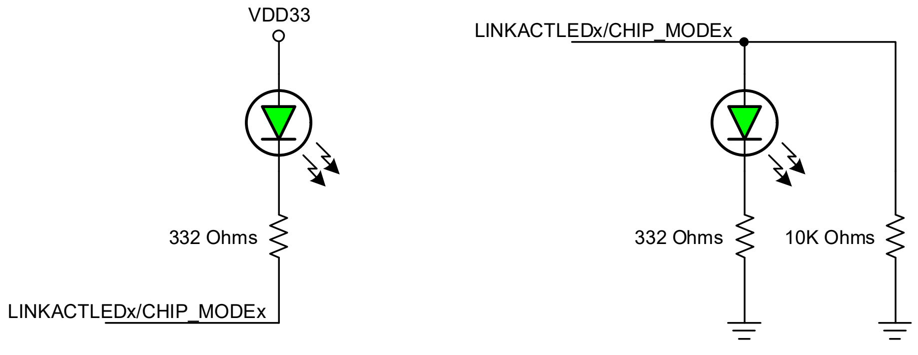


- **CHIP_MODE1** (pin 46) and **CHIP_MODE0** (pin 48) pins configure the number of active ports and port types of the LAN9253. The configuration modes are shown in Table 6-1, and the strapping is shown in Figure 6-3.

TABLE 6-1: LAN9253 MODE SELECTION

CHIP_MODE [1:0]	Mode
0x	2-Port mode: Port 0 = PHY A, Port 1 = PHY B Ports 0 and 1 are connected to internal PHYs A and B.
10	3-Port Downstream mode: Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII Ports 0 and 1 are connected to internal PHYs A and B. Port 2 is connected to the external MII pins.
11	3-Port Upstream mode: Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A Ports 2 and 1 are connected to internal PHYs A and B. Port 0 is connected to the external MII pins.

FIGURE 6-3: STRAPPING FOR LED/CHIP_MODEX



CHIP_MODEx Bit = 1

LED Output Signal from
LAN9253 is Active Low

CHIP_MODEx Bit = 0

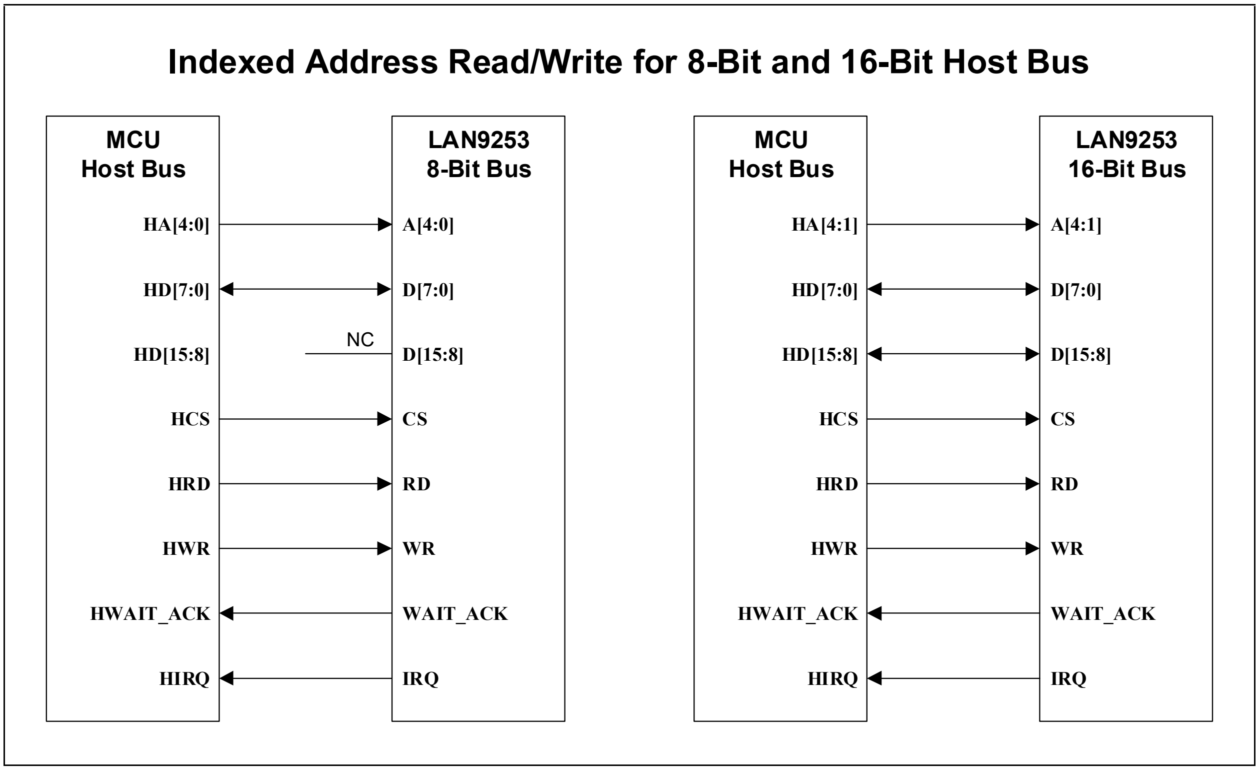
LED Output Signal from
LAN9253 is Active High

7.0 MICROCONTROLLER MODE VIA HOST BUS INTERFACE

7.1 Host Bus Interface Indexed Mode and Pins

The LAN9253 provides one 8-bit or 16-bit Indexed mode HBI. The connection between MCU and LAN9253 is shown in Figure 7-1.

FIGURE 7-1: CONNECTION BETWEEN LAN9253 AND MCU USING 8-BIT AND 16-BIT HBI



- **RD/RD_WR** (pin 31): The pin **RD** is the host bus read strobe. Normally active low, the polarity can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI modes). The **RD_WR** pin is the host bus direction control. Used in conjunction with the **ENB** pin, it indicates a read or write operation. The normal polarity is read when 1, and write when 0 but can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI modes).
- **WR/ENB** (pin 30): The **WR** pin is the host bus write strobe. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI modes). The **ENB** is the host bus data enable strobe. Used in conjunction with the **RD_WR** pin, it indicates the data phase of the operation. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI modes).
- The **CS** (pin 28) pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via the HBI Chip Select Polarity bit of the PDI Configuration Register (HBI modes).
- **A[4:0]** (pins 27, 26, 29, 25, and 33): These pins provide the address for non-multiplexed address mode. In 16-bit data mode, bit 0 is not used.
- **D[15:0]** (pins 33, 15, 16, 21, 22, 23, 19, 40, 39, 36, 50, 49, 35, 12, 13, and 17): These pins are the host bus data bus for non-multiplexed address mode. In 8-bit data mode, bits 15 to 8 are not used and their I/O drivers are disabled.

7.2 Host Bus Interface Multiplexed Mode and Pins

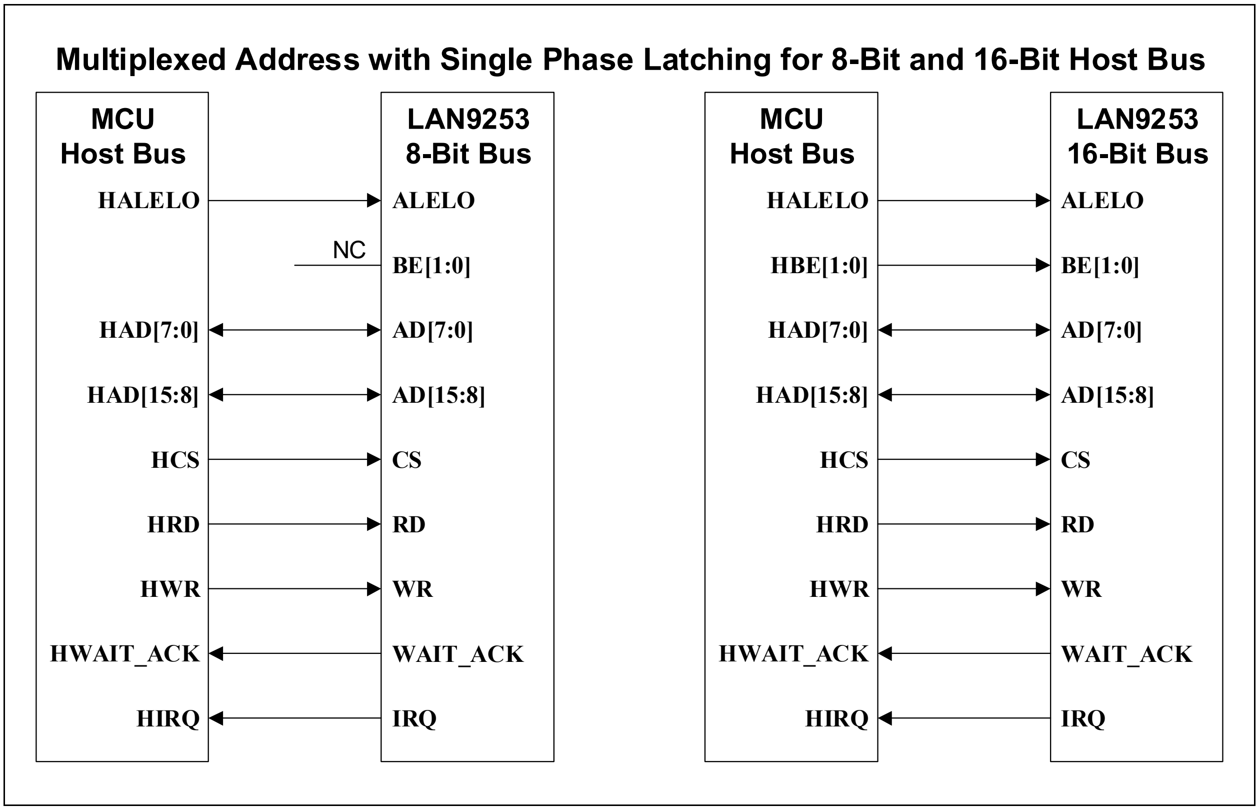
The LAN9253 provides one 8-bit or 16-bit Multiplexed mode HBI. The Multiplexed mode pins are described as follows, and the connections between MCU and LAN9253 are shown in Figure 7-2, Figure 7-3, and Figure 7-4.

- **RD/RD_WR** (pin 31): The **RD** pin is the host bus read strobe. Normally active low, the polarity can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI modes). The **RD_WR** pin is the host bus direction control. Used in conjunction with the **ENB** pin, it indicates a read or write operation. The normal polarity is read when 1, and write when 0 (R/nW) but can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI modes).
- **WR/ENB** (pin 30): The **WR** pin is the host bus write strobe. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI modes). The **ENB** pin is the host bus data enable strobe. Used in conjunction with the **RD_WR** pin, it indicates the data phase of the operation. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI modes).
- The **CS** (pin 28) pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via the HBI Chip Select Polarity bit of the PDI Configuration Register (HBI modes).
- **AD[15:0]** (pins 33, 15, 16, 21, 22, 23, 19, 40, 39, 36, 50, 49, 35, 12, 13, and 17): These pins are the host bus address/data bus for multiplexed address mode. Bits 15 to 8 provide the upper byte of address for single phase multiplexed address mode. Bits 7 to 0 provide the lower byte of address for single phase multiplexed address mode and both bytes of address for dual phase multiplexed address mode. In 8-bit data dual phase multiplexed address mode, bits 15 to 8 are not used and their I/O drivers are disabled.
- The **ALEHI** (pin 29) pin indicates the address phase for multiplexed address modes. It is used to load the higher address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI modes).
- The **ALELO** (pin 25) pin indicates the address phase for multiplexed address modes. It is used to load both address bytes in single phase multiplexed address mode and the lower address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI modes).

7.3 Multiplexed Address with Single Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address with single phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 7-2.

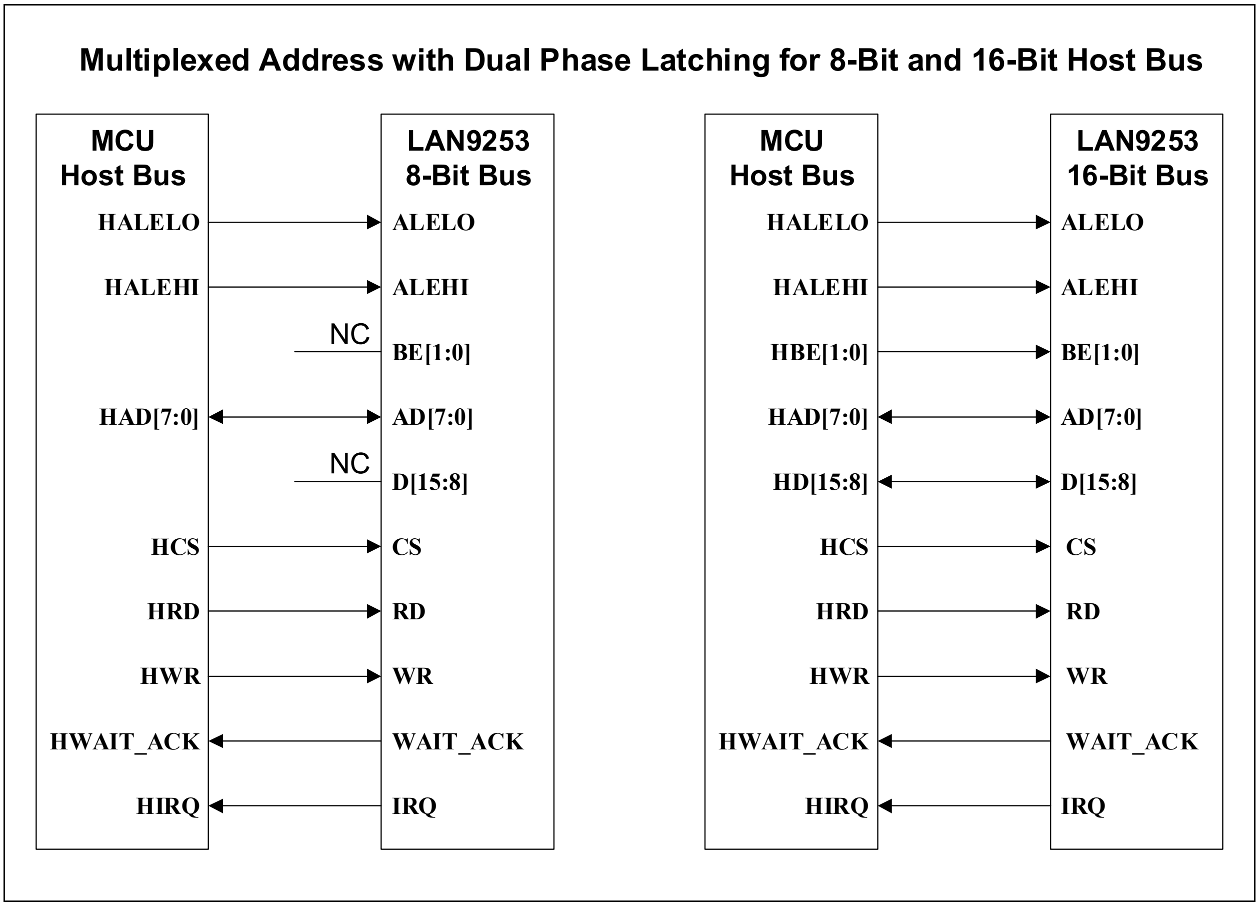
FIGURE 7-2: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS SINGLE PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



7.4 Multiplexed Address with Dual Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address with dual phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 7-3.

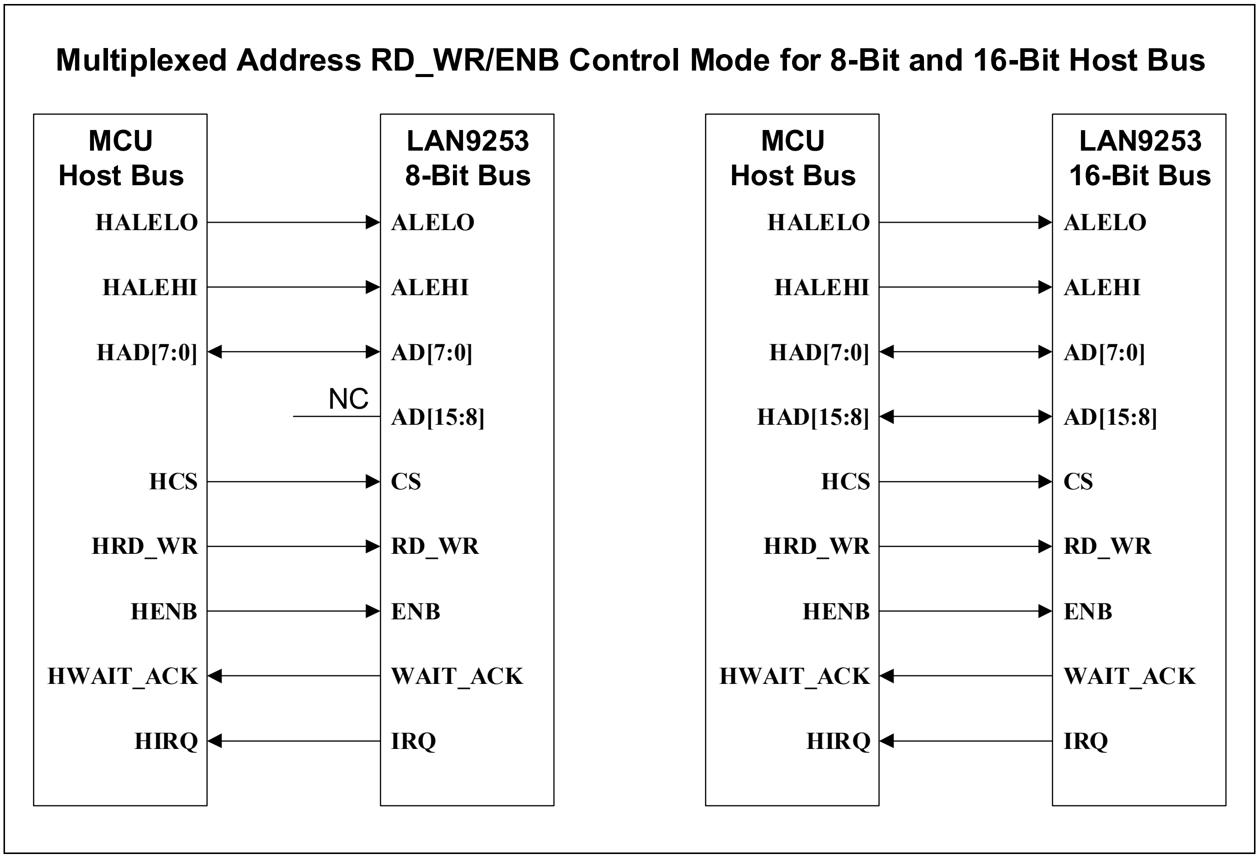
FIGURE 7-3: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS DUAL PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



7.5 Multiplexed Address RD_WR/ENB Control Mode for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address RD_WR/ENB control mode for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 7-4.

FIGURE 7-4: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HBI



8.0 MICROPROCESSOR/MICROCONTROLLER MODE VIA SPI/SQI INTERFACE

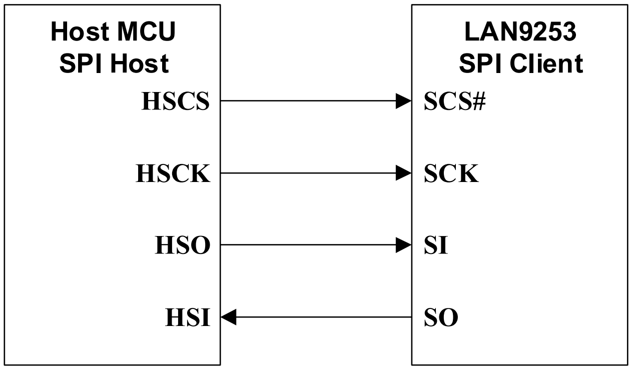
8.1 SPI/SQI Interface Pins

- The **SI** (pin 17) pin is the SPI Client serial data input. **SI** is shared with the **SIO0** pin. This input pin has an internal pull-up.
- The **SO** (pin 13) pin is the SPI Client serial data output. **SO** is shared with the **SIO1** pin. This output pin has an internal pull-up.
- The **SCK** (pin 19) pin is the SPI/SQI Client serial clock input. This input pin has an internal pull-up.
- The **SCS#** (pin 50) pin is the SPI/SQI Client chip select input. When low, the SPI/SQI Client is selected for SPI/SQI transfers. When high, the SPI/SQI serial data output(s) is tri-stated. This input has an internal pull-up.
- The **SIO[3:0]** (pins 35, 12, 13, and 17) pins are the SPI/SQI Client data input and output for multiple bit I/O. These bidirectional pins have internal pull-ups. **SIO0** is shared with the **SI** pin. **SIO1** is shared with the **SO** pin.

8.2 Using SPI Between Host MCU and LAN9253

- LAN9253 SPI/SQI interface supports up to an 80 MHz input clock.
- The connection between MCU SPI Host mode and LAN9253 SPI Client mode is shown in Figure 8-1.

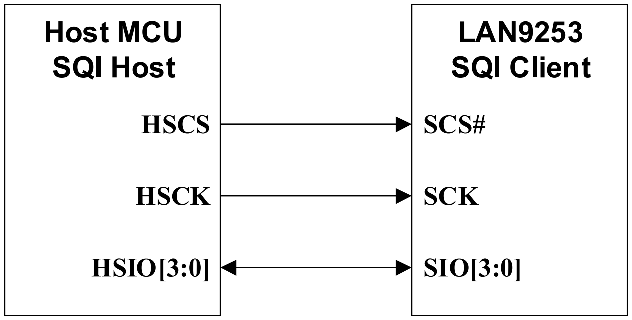
FIGURE 8-1: SPI CONNECTION BETWEEN MCU AND LAN9253



8.3 Using SQI Between Host MCU and LAN9253

The connection between MCU SQI Host mode and LAN9253 SQI Client mode is shown in Figure 8-2.

FIGURE 8-2: SQI CONNECTION BETWEEN MCU AND LAN9253



9.0 EXPANSION MODE WITH MII INTERFACE FOR EXTRA PORT

9.1 MII Signals and Connections

When utilizing either an external MII PHY or an MII connector, Table 9-1 indicates the proper connections for the 14 signals.

TABLE 9-1: LAN9253 MII SIGNALS TO EXTERNAL PHY OR MII CONNECTOR

From	Connects to	
LAN9253 QFN	**MII PHY Device**	**MII Connector**
RXD0 (pin 27)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 28)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 30)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 31)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 26)	RX_DV	RX_DV (contact 8)
RX_ER (pin 33)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 36)	RX_CLK	RX_CLK (contact 9)
—	TX_ER	TX_ER (contact 11)
TXD0 (pin 22)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 21)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 16)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 15)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 23)	TX_EN	TX_EN (contact 13)
—	TX_CLK	TX_CLK (contact 12)
—	CRS	CRS (contact 19)
—	COL	COL (contact 18)
MDIO (pin 40)	MDIO	MDIO (contact 2)
MDC (pin 39)	MDC	MDC (contact 3)

9.2 MII Interface for EtherCAT®

- **TX_CLK** from the external PHY is not connected since the EtherCAT Device controller does not incorporate a TX FIFO. The TX signals from the EtherCAT Device controller may be delayed with respect to the CLK25 output by using TX shift compensation so that they align properly as if they were driven by the TX_CLK of the PHY.
- The **COL** and **CRS** outputs from the PHY are not connected since EtherCAT operates in Full-duplex mode.
- The **TX_ER** input on the external PHY should be tied to system ground as the EtherCAT Device controller will never generate any transmit errors.

9.3 MII Interface Series Terminations

Provisions should be made for series resistors for all outputs on the MII/RMII interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN9253 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors are 22Ω. See Table 9-2.

TABLE 9-2: SERIES TERMINATIONS FOR MII INTERFACE

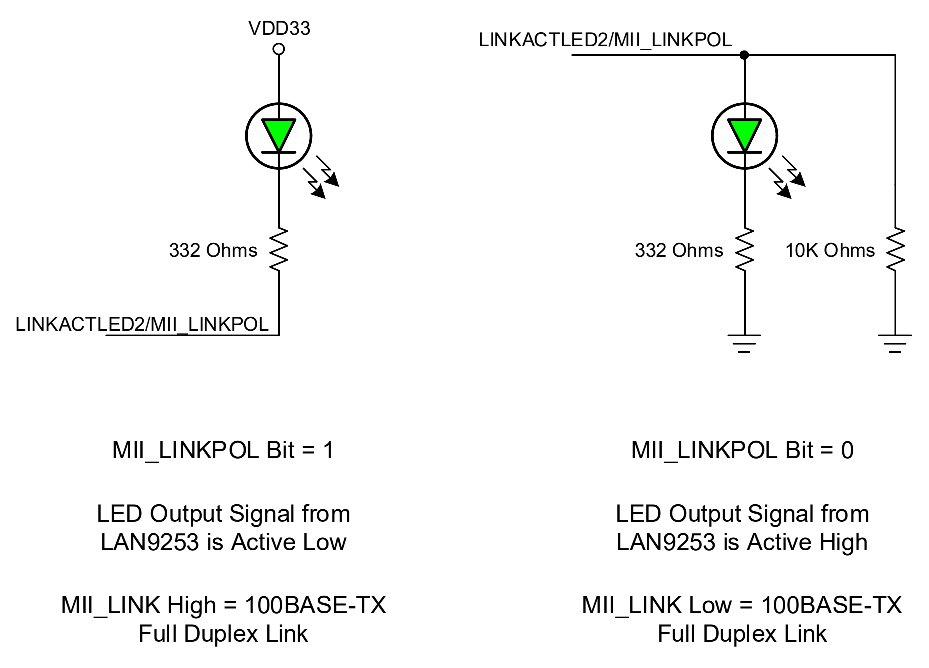
Signal Name	Series Resistors at LAN9253 Drive Pins	Series Resistors at External PHY Drive Pins
RXD [3:0]	—	22Ω
RXDV	—	22Ω
RXC	—	22Ω
RXER	—	22Ω
TXD [3:0]	22Ω	—
TXEN	22Ω	—

Note 1: The series resistors should be placed as close as possible to both devices MII drive pins in PCB layout.

9.4 Other Pins Related to MII Interface

- **MII_CLK25** (pin 25) is a free-running 25 MHz clock that can be used as the clock input to the external PHY.
- **MII_LINK** (pin 49) is an input pin on the LAN9253 is driven by the external PHY to indicate that a 100 Mbps full-duplex link is established. The polarity is configurable via the **MII_LINKPOL** strap.
- The **TX_SHIFT1** (pin 15) and **TX_SHIFT0** (pin 16) pins configure the value of the MII TX timing shift for the MII port of the LAN9253. The shift in timing are as follows:
  - 00: 20 ns
  - 01: 30 ns
  - 10: 0 ns
  - 11: 10 ns
- See the latest version of the *LAN9253 Data Sheet* for complete details. These pins have weak internal pull-ups and can be driven low with an external 4.7 kΩ resistor to system ground. If driven, these two input configuration strap pins require an external 4.7 kΩ pull-up resistor to ensure the proper high level is maintained.
- The **MII_LINKPOL** (pin 29) strap pin configures the polarity of the **MII_LINK** pin (pin 49). When latched low, **MII_LINK** low indicates a 100BASE-TX full-duplex link has been established. When latched high, **MII_LINK** high indicates a 100BASE-TX full-duplex link has been established. This pin has a weak internal pull-up and can be driven low with an external 1.0 kΩ resistor to system ground.

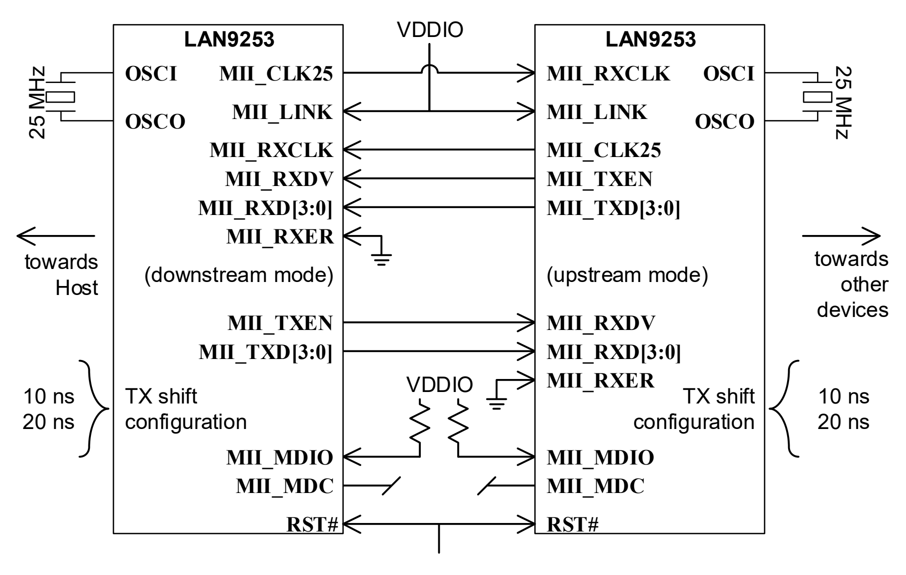
FIGURE 9-1: LED ACTIVE LOW/HIGH CIRCUITS



9.5 LAN9253 MII Back-to-Back Connections

- Two EtherCAT Device controllers can be connected using a back-to-back MII connection as shown in Figure 9-2. One device is placed in 3-Port Upstream mode, and the other in 3-Port Downstream mode.
- The clock sources of each EtherCAT Device controller may be different. The 25 MHz output (**MII_CLK25**) is provided to be used as the **RX_CLK** input to the other device.
- The TX signals from each EtherCAT Device controller may be delayed with respect to the CLK25 output by using TX shift compensation so that they align properly to meet the RX timing requirement of the other device.
- The MII_RXER signals are not used since the EtherCAT Device controllers never generate errors.

FIGURE 9-2: EtherCAT® Back-to-Back MII Connection



9.6 Placing and Routing in PCB Layout for MII Interface

- If the designer has determined that series terminations are required, they should be placed appropriately. Any series termination should be placed as close as possible to the associated driver of the MII signal.
- The MII interface on the LAN9253 should be constructed using 68Ω traces.
- The value of the series termination (if utilized) and the impedance of the internal driver of the LAN9253 should roughly equal that of the PCB trace impedance. The value of the series termination can be adjusted slightly to achieve the best signal integrity possible. (Using 22-33Ω series termination resistors is recommended.)
- If all traces lengths of the MII signals are matched to within 1.0”, the series termination resistors can be ignored due to the short traces have not formed the transmission line yet.

10.0 DIGITAL I/O MODE

The Digital I/O PDI provides 16 configurable digital I/Os (**DIGIO[15:0]**) to be used for simple systems without a host controller. The Digital I/O Output Data Register is used to control the output values, while the Digital I/O Input Data Register is used to read the input values. Each 2-bit pair of the digital I/Os is configurable as an input or output. The direction is selected by the Extended PDI Configuration Register, which is configured via EEPROM. The digital I/Os can also be configured to Bidirectional mode, where the outputs are driven and latched externally and then released so that the input data can be sampled. Bidirectional operation is selected via the Unidirectional/Bidirectional Mode bit of the PDI Configuration Register. The PDI Configuration Register is initialized from the contents of EEPROM.

10.1 Digital I/O Mode Pins

- The **SOF** (pin 12) pin is the Start of Frame output and indicates the start of an Ethernet/EtherCAT frame. Note that the signal is not driven (high impedance) until the EEPROM is loaded.
- The **EOF** (pin 13) pin is the End of Frame output and indicates the end of an Ethernet/EtherCAT frame. Note that the signal is not driven (high impedance) until the EEPROM is loaded.
- The **WD_STATE** (pin 17) pin is the SyncManager Watchdog State output. A 0 indicates the watchdog has expired. Note that the signal is not driven (high impedance) until the EEPROM is loaded.
- The **WD_TRIG** (pin 35) pin is the SyncManager Watchdog Trigger output. Note that the signal is not driven (high impedance) until the EEPROM is loaded.
- The **SYNC0/SYNC1** (pin 18/34) pins are the Distributed Clock Sync (OUT) signals.
- The **LATCH_IN** (pin 19) input pin is the external data latch signal. The input data is sampled each time a rising edge of LATCH_IN is recognized.
- The **OE_EXT** (pin 25) input pin is the Output Enable signal. When low, it clears the output data.
- The **OUT_VALID** (pin 50) pin indicates that the outputs are valid and can be captured into external registers. Note that the signal is not driven (high impedance) until the EEPROM is loaded.
- The **GPI[15:0]** (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, and 36) pins are the general purpose inputs and are directly mapped into the General Purpose Inputs Register.
- The **GPO[15:0]** (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, and 36) pins are the general purpose outputs and reflect the values of the General Purpose Outputs Register without watchdog protection.
- The **DIGIO[15:0]** (pins 31, 30, 28, 27, 26, 29, 33, 15, 16, 21, 22, 23, 49, 40, 39, and 36) pins are the input/output or bidirectional data. Note that these signals are not driven (high impedance) until the EEPROM is loaded.

10.2 Pins for Digital I/O Input Mode

Digital inputs can be configured to be sampled in four ways: at the start of each Ethernet frame EOF, at the rising edge of the **LATCH_IN** pin, at Distributed Clocks SYNC0 events, or at Distributed Clocks SYNC1 events. Details are shown in Table 10-1.

TABLE 10-1: ETHERCAT® DIGITAL I/O INPUT-RELATED PINS

Pin Name	Type	Description
SYNC0	VO8	The input data is sampled at the rising edge of SYNCO that is the Distributed Clock Synchronization (OUT) signal.
SYNC1	VO8	The input data is sampled at the rising edge of SYNCO that is the Distributed Clock Synchronization (OUT) signal.
LATCH_IN	VIS	External data latch signal that is sampled a rising edge of LATCH_IN
SOF	VO8	Indicate to start an Ethernet/EtherCAT frame
GPI[15:0]	VIS/VO8	General purpose inputs and are directly mapped into the General Purpose Inputs Register.

10.3 Pins for Digital I/O Output Mode

Digital outputs can be configured to be updated in four ways: at the end of each Ethernet frame, with Distributed Clocks SYNC0 events, with Distributed Clocks SYNC1 events, or at the end of an EtherCAT frame that triggered the Process Data Watchdog. The choice of sampling mode is determined by the Output Data Sample Selection bits of the PDI Configuration Register that is initialized from the contents of EEPROM. Details are shown in Table 10-2.

TABLE 10-2: ETHERCAT® DIGITAL I/O OUTPUT-RELATED PINS

Pin Name	Type	Description
SYNC0	VO8	The output data is sampled at the rising edge of SYNCO
SYNC1	V08	The output data is sampled at the rising edge of SYNC1
EOF	VO8	The End of Frame output and indicates the end of an Ethernet/EtherCAT frame
WD_TRIG	VO8	Output data is updated if watchdog is triggered on OUTVALID mode
OUTVALID	VO8	Indicates the outputs are valid and can be captured into registers
OE_EXT	VIS	It is the Output Enable input. When low, it clears the output data.
GPO[15:0]	VIS/VO8	General purpose outputs and reflect the values of the General Purpose Outputs Register

10.4 Pins for Digital I/O Bidirectional Mode

Digital I/O input or output direction depends on the output polarity of the **OUTVALID** pin (Low is for input, High is for output) determined by the OUTVALID Polarity bit of the PDI Configuration Register, which is initialized from the contents of EEPROM. The default value of this field can be configured via EEPROM. Details are shown in Table 10-3.

TABLE 10-3: ETHERCAT® DIGITAL I/O BIDIRECTIONAL-RELATED PINS

Pin Name	Type	Description
OUTVALID	VO8	Indicates the outputs are valid and can be captured into registers.
DIGIO[15:0]	VIS/VO8	16 configurable digital I/O data input or output

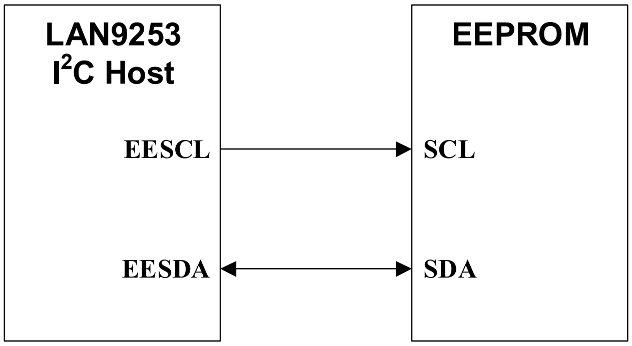
11.0 EEPROM INTERFACE

The LAN9253 contains an I^2C Host controller, which uses the **EESCL** and **EESDA** pins. **EESCL** and **EESDA** require an external pull-up resistor. Both 1 byte and 2 byte addressed EEPROMs are supported. The size is determined by the **E2PSIZE** configuration strap.

11.1 EEPROM Pins

- **EESDA** (pin 42): When the device is accessing an external EEPROM, this pin is the I^2C serial data input/open-drain output. Note that this pin must be pulled-up by a 10 kΩ external resistor at all times.
- **EESCL** (pin 43): When the device is accessing an external EEPROM, this pin is the I^2C clock open-drain output. Note that this pin must be pulled-up by a 10 kΩ external resistor at all times.
- For EtherCAT operation, an EEPROM is required. Please review the “EEPROM Configurable Register” section in the *LAN9253 Data Sheet* for the specific design functionality is loaded from the EEPROM.
- The connection as shown in Figure 11-1.

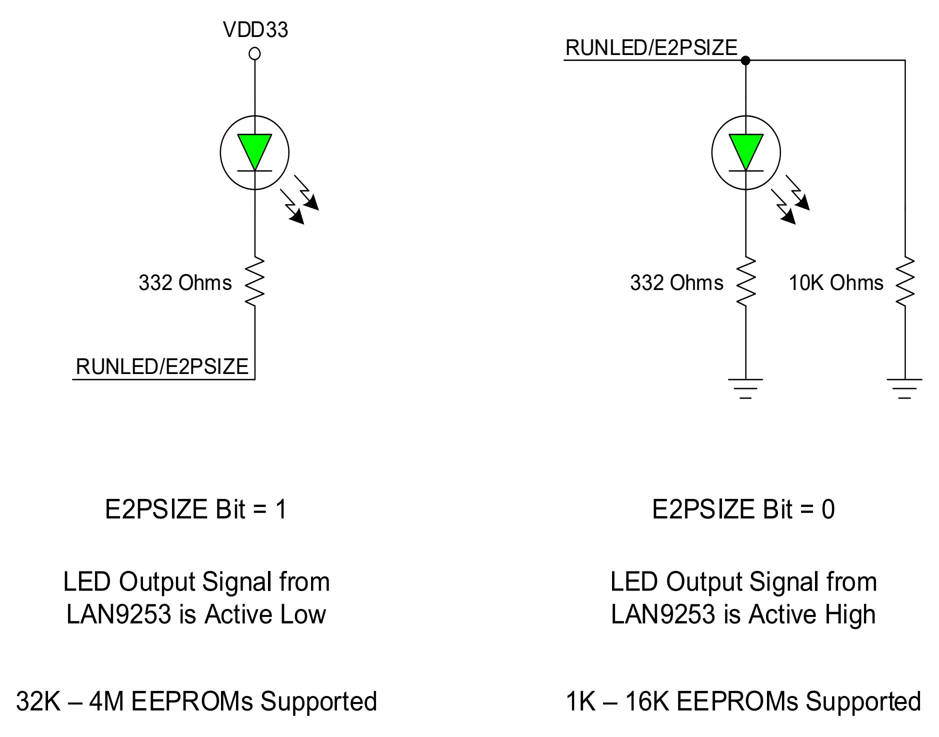
FIGURE 11-1: CONNECTION BETWEEN LAN9253 AND EEPROM (1/2)



11.2 EEPROM Related Strapping Pin

- **E2PSIZE** (pin 45): This strap pin configures the I^2C EEPROM size.
- When latched low, EEPROM sizes 128 x 8-bit (1K) through 2048 x 8-bit (16K) are supported.
- When latched high, EEPROM sizes 4096 x 8-bit (32K) through 512K x 8-bit (4M) are supported.
- This pin has a weak internal pull-up and can be driven low with an external 1.0 kΩ resistor to system ground.
- The connection as shown in Figure 11-1.

FIGURE 11-2: CONNECTION BETWEEN LAN9253 AND EEPROM (2/2)



11.3 EEPROM Emulation Mode

- LAN9253 can be configured to EEPROM Emulation mode to reduce the system cost.
- Configure pin 43 **EE_EMUL2** or pin 42 **EE_EMUL1** strap low to enable EEPROM Emulation mode.
- For normal EEPROM operation, the **EE_EMUL2** or **EE_EMUL1** configuration straps should include an external pull-up.
- Strap pins [43, 42, and 45], EE_EMUL [2:0] to get different modes:
  - 000: SPI
  - 001: HBI Indexed 16-bit EtherCAT Direct Mapped
  - 010: HBI Multiplexed 1 Phase 16-bit EtherCAT Direct Mapped
  - 011: HBI Multiplexed 2 Phase 16-bit EtherCAT Direct Mapped
  - 100: SPI EtherCAT Direct Mapped
  - 101: Beckhoff SPI mode
  - 110: N/A (EEPROM is enabled)
  - 111: N/A (EEPROM is enabled)
- Normally, all host interfaces (HBI and SPI) are disabled, since much of the device is configured by the EEPROM contents.
- When EEPROM Emulation mode is used, a host interface configuration must be selected in order to allow the host microprocessor to access the EEPROM registers.
- In EEPROM Emulation mode, the software can emulate EEPROM Host to access LAN9253 EEPROM registers.

12.0 ETHERNET/ETHERCAT® LED INDICATORS

There are LEDs for Ethernet/EtherCAT port 0, port 1, and port 2.

12.1 Port LED Pins

- **LINKACTLED0** (pin 48): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 0 (Port A). This pin is configured to be open-drain/open-source output. The choice of open-drain against open-source, as well as the polarity of this pin, depends upon the strap value sampled at reset.
- **LINKACTLED1** (pin 46): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 1 (Port B). This pin is configured to be open-drain/open-source output. The choice of open-drain against open-source, as well as the polarity of this pin, depends upon the strap value sampled at reset.
- **LINKACTLED2** (pin 29): This pin is the Link/Activity LED output (off = no link, on = link without activity, blinking = link and activity) for Port 2. This pin is configured to be an open-drain and open source output. The choice of open-drain against open source, as well as the polarity of this pin, depends upon the strap value sampled at reset.

12.2 Other LED-Related Pins

- **RUNLED/STATE_RUNLED** (pin 45): This pin is the Run LED output and is controlled by the AL Status Register. This pin is configured to be open-drain/open-source output. The choice of open-drain against open-source, as well as the polarity of this pin, depends upon the strap value sampled at reset.
- **STATE_RUNLED**: This is an output pin, which is equal to the **RUNLED** combined with the negation of the **ERRLED**. It can be used to control the RUN side of a bicolor **RUNLED/ERRLED**.
- **ERRLED/PME/100FD_B/LEDPOL4** (pin 9) is the configuration strap-in to select the different function. There are four cases as below:
  - **ERRLED** is enabled via the EEPROM contents and should be set to disabled. In the event of an EEPROM loading error, the ERRLED function is forced enabled and false PME events might occur. ERRLED is controlled either by the EtherCAT Device controller or by the local MCU. If ERRLED is needed, the pin should connect to an external LED through a current limit resistor as error LED.
  - If the design has PME wake-up interrupt feature, the pin as **PME** can be connected to one of the MCU GPIO pin. Selecting pin 9 as PME depends on the Power Management Control Register (PMT_CTRL) bits [9:7].
  - **100FD_B**: Pin 9 can also be used as a strap pin for the port B (port 1) in 3-Ports mode for Auto-Negotiation and Auto-MDIX disable/enable.

    0: Auto-negotiation and AMDIX enabled by default

    1: Auto-negotiation and AMDIX disabled (Force 100 Mbps full duplex) by default.

    In 2-Ports mode, this strap is on the **ERRLED** pin.
  - **LEDPOL4**: For LED 4 Polarity configuration strap-in pin, check the strap setting based on design and the following:

    0: The LED is set as active high by default.

    1: The LED is set as active low by default.

13.0 MISCELLANEOUS

13.1 Other Important Pin Settings

- **RBIAS** (pin 57) on the LAN9253 should connect to the system ground through a 12.1 kΩ resistor with a tolerance of 1.0%. The **RBIAS** pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical devices.
- **RST#** (pin 11): As an input, this active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus this signal may be left unconnected if an external hardware reset is not needed. When used, this signal must adhere to the reset timing requirements as detailed in the “Operational Characteristics” section of the data sheet. As an output, this signal is driven low during POR or in response to an EtherCAT reset command sequence from the Host controller or Host interface.
- The **REG_EN** (pin 7) pin enables or disables the two +1.2V internal regulators of the LAN9253. Refer to the latest revision of the data sheet for additional information. Connecting this pin to +3.3V will enable the regulators. Connecting this pin to system ground will disable both regulators. This pin has no internal terminations and must be strapped accordingly.
- The LAN9253 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board-level testing to ensure system functionality and board manufacturability. For details, see the *LAN9253 Data Sheet*.
- **TESTMODE** (pin 41): This input pin must be tied to VSS system ground to ensure proper operation.
- To take advantage of the JTAG interface, the **TESTMODE** pin must be driven high. Then, for normal operation, the **TESTMODE** pin must be driven low. This pin has an internal pull-down to ensure normal operation as a No Connect (NC).
- **IRQ** (pin 44) Interrupt request output: The polarity, source, and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to the “System Interrupts” section of the data sheet.
- Configuration strap values are typically latched on power-on reset and system reset. Microchip will guarantee that the proper high/low level will be latched in on any device pin with an internal pull-up or pull-down where the device pin is a true No Connect. However, when the configuration strap pin (typically an output pin) is connected to a load, the input leakage current associated with the input load may have an adverse effect on the high/low level ability of the internal pull-up/pull-down. In this case, Microchip recommends to include an external resistor to augment the internal pull-up/pull-down to ensure the proper high/low level for configuration strap values. Lower VDDIO voltages will further exacerbate this condition.
- The recommended pull-up and pull-down resistors values for strap pins are 4.7 kΩ and 1 kΩ, respectively for the general strap pins.
- Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far away from LAN9253 device in PCB layout placement for better ESD.

13.2 Placing and Routing in PCB Layout for Other Pins

- Place the RBIAS resistor as close to pin 57 of the LAN9253 QFN as possible.
- There are no components placement issues associated with the pull-up/down resistors, HBI, Digital I/O, SPI/SQI, LED, and EEPROM.
- The **RBIAS** resistor (pin 57) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the RBIAS resistor.
- There are no critical routing instructions for the pull-up/down resistors, HBI, Digital I/O, SPI/SQI, LED, and EEPROM.
- Microchip recommends utilizing at least a four-layer design for boards for the LAN9253 QFN device. The design engineer should be aware, however, that as tighter EMC standards are applied to the product and as faster signal rates are utilized by the design, the product design may benefit by utilizing up to eight layers for the PCB construction.
- As with any high-speed design, the use of series resistors and AC terminations is very application-dependent. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

- Bulk capacitors for each power plane should be routed immediately into power planes with traces as short and wide as possible.
- Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.
- Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, and so on). The electrical engineer must work with the PCB designer to determine all these variables.

14.0 HARDWARE CHECKLIST SUMMARY

TABLE 14-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet and Table 2-1.		
Section 3.0, "Power"	Section 3.1, "+3.3V Power Supply Connections"	Check the connection and design based on this section request in the schematics design for 3.3V power.		
	Section 3.2, "+1.8V to +3.3V Variable I/O Power Supply Connections"	Check the connection and design based on this section request in the schematics design for VDDIO power		
	Section 3.3, "VDDCR"	Check the connection and design based on this section request in the schematics design for VDDCR power based on internal 1.2V regulators Enable mode or Disable mode.		
	Section 3.4, "Power and Ground Connections"	Check the connection and design based on Figure 3-1 and Figure 3-2 for the Regulator Enable mode or the Regulator Disabled mode.		
	Section 3.5, "Placing Power Pins in PCB Layout"	If going into PCB layout stage, check the components placement based on this section requirement for power.		
	Section 3.6, "Routing Power Pins in PCB Layout"	If going into PCB layout stage, check the traces routing based on this section requirement for power.		
Section 4.0, "Ethernet/EtherCAT® Signals"	Section 4.1, "LAN9253 Copper Port A Differential Pair PHY Interface"	Check if port A design and connection correct for 49.9Ω termination resistors on TX and RX pairs and analog 3.3V power based on Figure 4-1 and Figure 4-2 and this section requirement.		
	Section 4.2, "LAN9253 Copper Port B Differential Pair PHY Interface"	Check if port B design and connection correct for 49.9Ω termination resistors on TX and RX pairs and analog 3.3V power based on Figure 4-1 and Figure 4-2 and this section requirement.		
	Section 4.3, "LAN9253 Copper Port A Differential Pair PHY Magnetics"	Check if port A design and connection correct for the primary of magnetics and the secondary of magnetics with 75Ω resistor through a 1000 pF, 2 kV capacitor based on Figure 4-1 and Figure 4-2 and this section requirement.		
	Section 4.4, "LAN9253 Copper Port B Differential Pair PHY Magnetics"	Check if port B design and connection correct for the primary of magnetics and the secondary of magnetics with 75Ω resistor through a 1000 pF, 2 kV capacitor based on Figure 4-1 and Figure 4-2 and this section requirement.		
	Section 4.5, "LAN9253 Port A and Port B Differential Pair Between Magnetics and RJ45"	Check if termination is correct for the unused pins pairs 4/5 and 7/8 of RJ45 connector based on this section requirement.		
	Section 4.6, "Using RJ45 with Integrated LED"	Use RJ45 with integrated LED if the product working environment is not very noisy. Otherwise, use an independent LED solution.		
	Section 4.7, "Placing Copper Ports in PCB Layout"	If going into PCB layout stage, check the components placement based on Figure 4-3 and this section requirement for the copper ports.		
	Section 4.8, "Routing Copper Ports in PCB Layout"	If going into PCB layout stage, check the traces routing based on this section requirement for the copper ports.		

TABLE 14-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal or Oscillator Clock Connections"	Verify the usage of 25 MHz max. ±50 ppm crystal. The drive level should be minimum 50 uW, typical 300 uW above (preferably higher). If using 25 MHz oscillator with maximum ±50 ppm, it is better to use 3.3V power oscillator. The design and connection is based on Figure 5-1 and this section requirement.		
	Section 5.2, "Other Clock Pins"	If additional 25 MHz clock output is needed for other device, check this section. Otherwise, ignore this section.		
	Section 5.3, "Placing and Routing Crystal in PCB Layout"	If going into PCB layout stage, check the components placement and traces routing based on this section requirement for crystal/oscillator circuit.		
Section 6.0, "Configuration for System Applications"	Section 6.1, "Microcontroller Mode with Host Bus Interface"	Check to see if your system design fits this mode and refer to Figure 6-1		
	Section 6.2, "Microcontroller Mode with SPI/SQI Interface"	Check to see if your system design fits this mode and refer to Figure 6-1.		
	Section 6.3, "Expansion Mode with MII to External PHY"	Check to see if your system design fits this mode and refer to Figure 6-1.		
	Section 6.4, "Digital I/O Mode"	Check to see if your system design fits this mode and refer to Figure 6-1.		
	Section 6.5, "System Block Diagram"	Check if is correct system design for 2-Port mode, 3-Port Downstream mode, and 3-Port Upstream mode, and correct strapping for the system configuration.		
Section 7.0, "Microcontroller Mode Via Host Bus Interface"	Section 7.1, "Host Bus Interface Indexed Mode and Pins"	If design uses HBI Indexed mode, please check 8-bit or 16-bit host bus connection based on Figure 7-1 and this section requirement.		
	Section 7.2, "Host Bus Interface Multiplexed Mode and Pins"	For (HBI) Multiplexed mode pins and connection, make sure input and output connections are correct between MCU and LAN9253.		
	Section 7.3, "Multiplexed Address with Single Phase Latching for 8-Bit and 16-Bit Host Bus Interface"	If design uses HBI Multiplexed Address with Single Phase Latching mode, please check 8-bit or 16-bit host bus connection based on Figure 7-2 and this section requirement.		
	Section 7.4, "Multiplexed Address with Dual Phase Latching for 8-Bit and 16-Bit Host Bus Interface"	If design uses HBI Multiplexed Address with Dual Phase Latching mode, please check 8-bit or 16-bit host bus connection based on Figure 7-3 and this section requirement.		
	Section 7.5, "Multiplexed Address RD_WR/ENB Control Mode for 8-Bit and 16-Bit Host Bus Interface"	If design uses HBI Multiplexed Address RE_WR/ENB Control mode, please check 8-bit or 16-bit host bus connection based on Figure 7-4 and this section requirement.		
Section 8.0, "Microprocessor/ Microcontroller Mode Via SPI/ SQI Interface"	Section 8.1, "SPI/SQI Interface Pins"	For MCU via SPI/SQI mode pins and connection, make sure input and output connections are correct between MCU and LAN9253.		
	Section 8.2, "Using SPI Between Host MCU and LAN9253"	If design uses SPI interface, please check SPI interface connection based on Figure 8-1 and this section requirement.		
	Section 8.3, "Using SQI Between Host MCU and LAN9253"	If design uses SQI interface, please check SQI interface connection based on Figure 8-2 and this section requirement.		

TABLE 14-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Expansion Mode with MII Interface for Extra Port"	Section 9.1, "MII Signals and Connections"	If design uses Expansion mode with MII interface, please check MII interface connection with external PHY based on Table 9-1 and this section requirement.		
	Section 9.2, "MII Interface for EtherCAT®"	For EtherCAT MII, please check pins of **TX_CLK**, **COL**, **CRS**, and **TXER** for correct design based on this section requirement.		
	Section 9.3, "MII Interface Series Terminations"	Check if all drive pins have the series termination resistors on MII interface based on Table 9-2 and this section requirement.		
	Section 9.4, "Other Pins Related to MII Interface"	Check if MII related strap pins setting based on Figure 9-1 and this section requirement.		
	Section 9.5, "LAN9253 MII Back-to-Back Connections"	If two LAN9253 device for MII back-to-back connection are needed, check if is correct based on Figure 9-2.		
	Section 9.6, "Placing and Routing in PCB Layout for MII Interface"	If going into PCB layout stage, check the components placement and traces routing based on this section requirement for MII interface.		
Section 10.0, "Digital I/O Mode"	Section 10.1, "Digital I/O Mode Pins"	When using digital I/O mode pins and connection, make sure correct pins are used, and the input and output are connected correctly.		
	Section 10.2, "Pins for Digital I/O Input Mode"	If the design uses Digital I/O Input mode, refer to Table 10-1 in the design.		
	Section 10.3, "Pins for Digital I/O Output Mode"	If the design uses Digital I/O Output mode, refer to Table 10-2 in the design.		
	Section 10.4, "Pins for Digital I/O Bidirectional Mode"	If the design uses Digital I/O Bidirectional mode, refer to Table 10-3 in the design.		
Section 11.0, "EEPROM Interface"	Section 11.1, "EEPROM Pins"	If design use EEPROM, check EEPROM connection based on Table 9-1 and this section requirement.		
	Section 11.2, "EEPROM Related Strapping Pin"	Check EEPROM related strap pin setting for correct EEPROM size used based on Figure 11-2.		
	Section 11.3, "EEPROM Emulation Mode"	If the design without using EEPROM and use EEPROM Emulation mode, check the EEPROM strap pins to enable EEPROM Emulation mode and correct setting.		
Section 12.0, "Ethernet/EtherCAT® LED Indicators"	Section 12.1, "Port LED Pins"	Check if use LED correct for each copper port.		
	Section 12.2, "Other LED-Related Pins"	Check other LED related strap pins to see if set correct.		
Section 13.0, "Miscellaneous"	Section 13.1, "Other Important Pin Settings"	Check other important pins setting correctly. For example, RBIAS resistor must be use 12.1KΩ resistor, RST# pin, REG_EN pin and so on based on this section requirement.		
	Section 13.2, "Placing and Routing in PCB Layout for Other Pins"	If go into PCB layout stage, check the components placement and traces routing based on this section requirement for these pins.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003644B (11-05-20)	Section 5.1, "Crystal or Oscillator Clock Connections"	Updated the information for **OSCO** pin, and updated Figure 5-1.
	Section 9.4, "Other Pins Related to MII Interface"	Corrected the TX timing shift values.
DS00003644A (09-30-20)	Initial release	

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication is provided for the sole purpose of designing with and using Microchip products. Information regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL OR CONSEQUENTIAL LOSS, DAMAGE, COST OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.
The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.
GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-7087-8

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820