Clock and Timing

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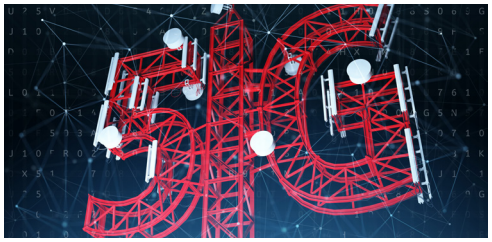
Complete Timing and Synchronization Solutions for 5G



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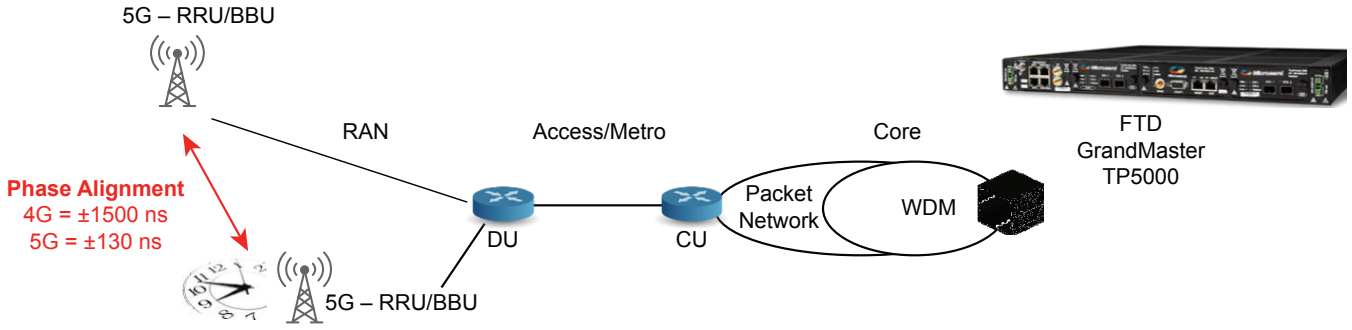
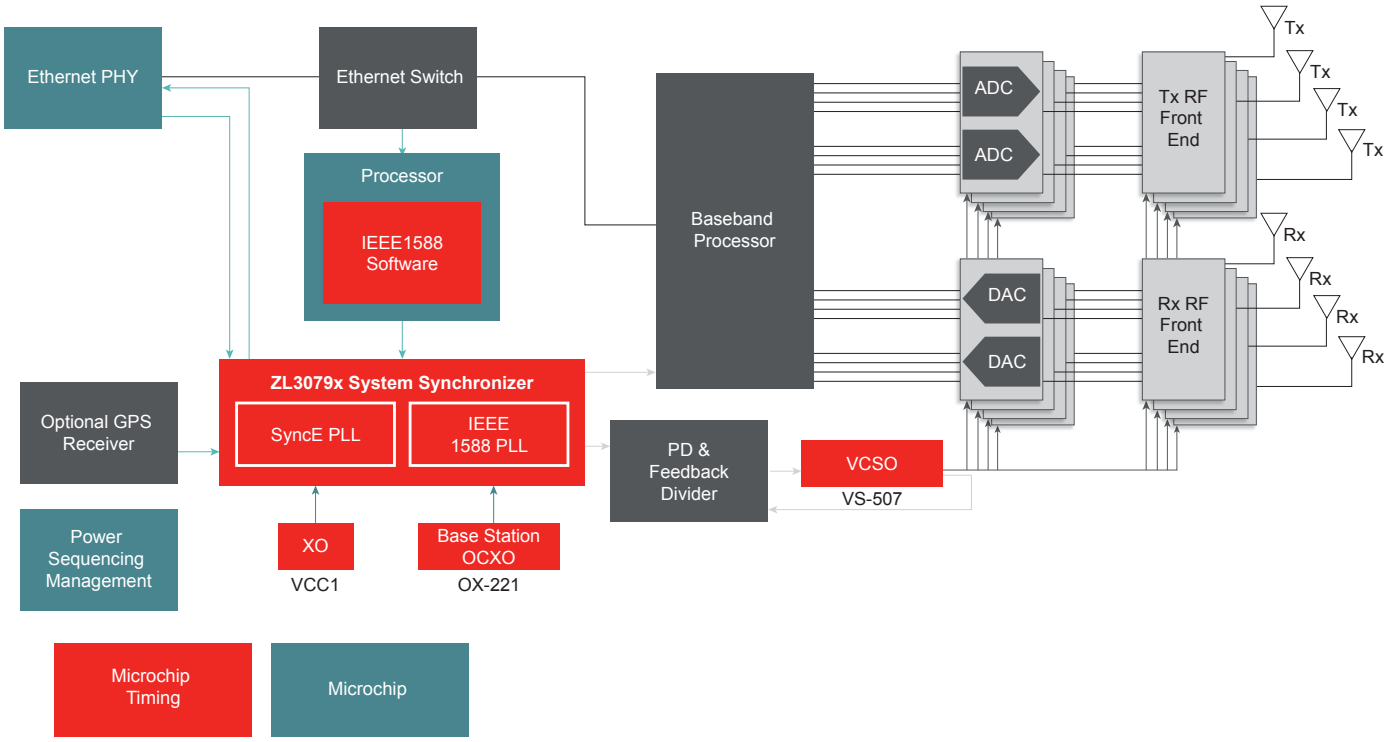
5G is Radically Changing the Network Synchronization Landscape



- **Requirements:** Moving from frequency to time with tight accuracy requirement down to 130 ns from 4Gs 1500 ns
- **Technology:** Multiple technologies are being used to achieve the required performance from GPS to SyncE & IEEE1588
- **Holdover:** More critical to have diverse synchronization sources and strong holdover
- **Connectivity:** Moving from CPRI/proprietary to eCPRI/25G
- **White Boxes:** Starting to see white box designs for 5G (OpenCompute)

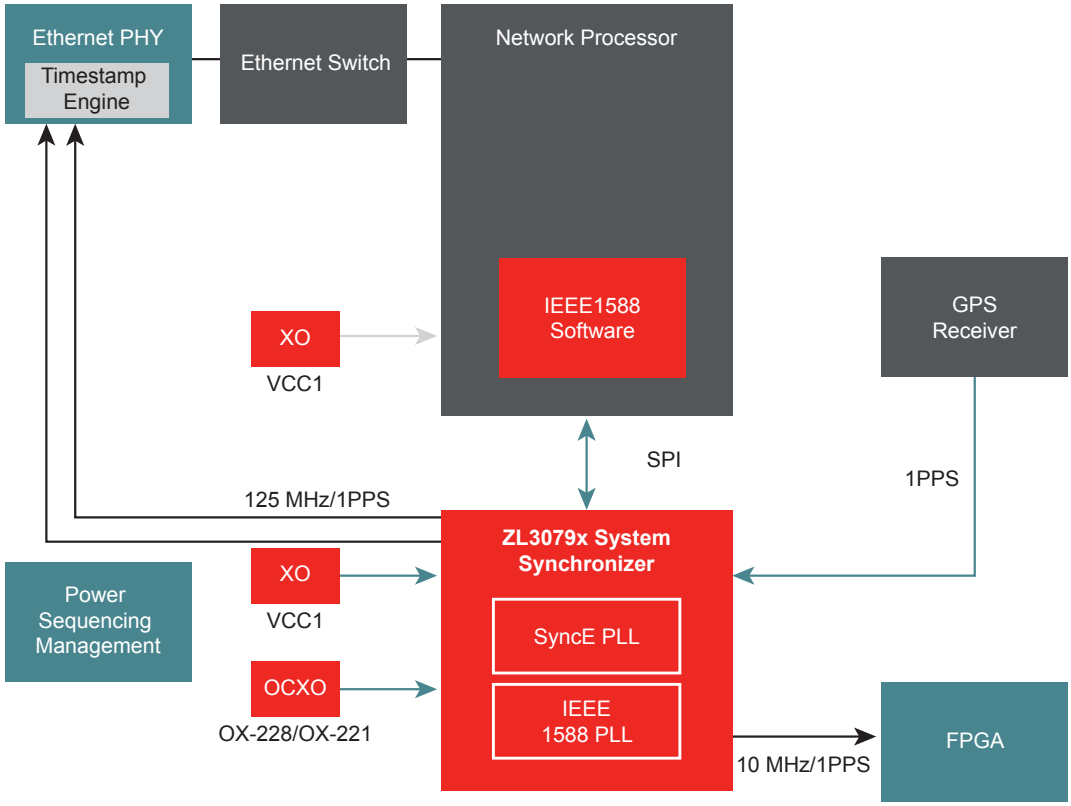
Radio Unit (RU)/Basestation



Key Problem Solved

- Support for IEEE1588, SyncE and GPS independent clock domains
- Compliance to G.8273.2 class C and D as part of T-TSC (Telecom Time Slave Clock), G.8262 and G8262.1 EEC/SyncE (Electrical Equipment Clock) and traceability to GPS clock domains
- OCXO temperature range up to 95°C and I^2C interface to use external compensation

Distributed Unit (DU)/Central Unit (CU)



Key Problem Solved

- Support for IEEE1588, SyncE and GPS independent clock domains
- Compliance to G.8273.2 class C and D as part of T-BC (Telecom Boundary Clock), G.8262 and G8262.1 EEC/SyncE (Electrical Equipment Clock) and traceability to GPS clock domains
- OCXO with <2 ppb temperature stability, <8 µsec holdover, and 95°C

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Oscillators

Model	Type	Footprint (mm)	Output Frequencies (MHz)	Temperature Stability (ppb)	Temperature Range (°C)	Supply Voltage (V)	Key Feature
OX-601	OCXO	9 × 7	10–40	10	–40 to 105	3.3	Small Footprint, Low power
OX-502	OCXO	14 × 9	10–40	10	–40 to 105	3.3	Small Footprint, Low power
OX-221	OCXO	25 × 22	10–30.72	3	–40 to 85	3.3	Good Holdover Performance
OX-228	OCXO	25 × 22	10–20	1	–40 to 85	3.3	Excellent Holdover Performance
OX-401	OCXO	20 × 13	10–40	5	–40 to 95	3.3	Excellent Wander (MTIE & TDEV)
MX-503	MCXO	14 × 9	10, 12.8, 20	50	–40 to 105	3.3	Very-Low Power
MX-700	MCXO	14 × 9	10–40	30	–40 to 105	3.3	Very-Low Power
VT-803	TCXO	5 × 3.2	10, 12.8, 20	280	–40 to 95	2.5, 3.3, 5	Low Power
VCC1	XO	7 × 5	49.152	50000	–40 to 85	3.3	Low Jitter
VS-505	VCXO	14 × 9	122–491	50000	–40 to 105	3.3	Ultra-Low Phase Noise
VS-805	VCXO	5 × 3.1	122–245	50000	–40 to 105	3.3	Ultra-Low Phase Noise
VS-507	VCSO	14 × 9	3000–6000	200000	–40 to 85	3.3	Ultra-Low Jitter

Clock Management

Model	Type	Number of Outputs	Output Logic	Jitter	Features
SM803	Low Jitter Clock Generator	12	CMOS, PECL, LVDS, HCSL	180 fs Phase Jitter @156.25 MHz (12KHz to 20MHz)	AnyRate Clock Generation with 12 programmable outputs up to 850 MHz
SM806	Ultra-Low Jitter Clock Generator	6	CMOS, PECL, LVDS, HCSL	78 fs Typ, 100 fs Max Phase jitter @ 156.25MHz (12KHz to 20MHz)	AnyRate Clock Generation with 6 programmable outputs up to 875 MHz
ZL3026x	Configurable Clock Generator	10	LVDS, LVPECL, HCSL, 2xCMOS or HSTL	170 fs (integer divider), 500 fs (fractional divider)	8 pin-selectable custom configurations 2 fractional PLLs plus fractional and integer dividers give up to 10 different frequencies in 4 frequency families – Clock Tree on a Chip
ZL3025x	Jitter Attenuator	3 Diff 6 CMOS	CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL	250 fs Phase Jitter @ 156.25 MHz (12 kHz to 20 MHz)	Low BW jitter filtering >14Hz cleans reference clock with glitchless switching Any-to-any frequency conversion - multiply low frequency clocks <1Hz
ZL4023x	Configurable Fanout Buffer	Up to 10	LVPECL, LVDS, HCSL, LVCMOS	50 fs Additive Jitter @ 156.25 MHz (12 kHz to 20 MHz)	3 to 1 input Multiplexer with pin control Pin control of output formats SPI control of output frequencies
MX87	Ultra-Low Jitter Clock Generator	6	CMOS, PECL, LVDS, HCSL	78 fs Typ, 100 fs Max Phase jitter @ 156.25MHz (12KHz to 20MHz)	Single ship solution with integrated Crystal, AnyRate Clock Generation with 6 programmable outputs up to 875 MHz

Model	Type	Footprint	Output Frequencies	Temperature Stability	Temperature Range	Supply Voltage	Key Featurs
MX77	XO	5 × 7	12.5–875	50000	–40°C to +85°C	2.5, 3.3	100 fs max Phase Jitter 12 KHz to 20 MHz

SyncE/IEEE1588

Part #	Application	# of Channels	DPLLs Can Be NCO	DPLL BW (Hz)	Inputs	Outputs	# of Freq Families	Typ/Max Jitter fs RMS	Input Freq. Range (Hz)	Output Freq. Range (Hz)	Pkg. Size (mm)
ZL30661	SyncE Line Card	1	1	14–470	5D/10S	8D/16S+2S	5	230/300	1k–900M	0.5–1045M	11x11
ZL30662	SyncE Line Card	2	2	14–470	5D/10S	8D/16S+2S	5	230/300	1k–900M	0.5–1045M	11x11
ZL30663	SyncE Line Card	3	3	14–470	5D/10S	8D/16S+2S	5	230/300	1k–900M	0.5–1045M	11x11
ZL30691	SyncE Timing Card	1	1	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11
ZL30692	SyncE Timing Card	2	2	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11
ZL30693	SyncE Timing Card	3	3	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11
ZL30791	SyncE/IEEE1588	1	1	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11
ZL30795	SyncE/IEEE1588	2	2	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11
ZL30793	SyncE/IEEE1588	3	3	0.1m–470	5D/10S	8D/16S+2S	5	230/300	0.5–900M	0.5–1045M	11x11

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