EVB-LAN9252-3PORT EtherCAT® ESC PHY Connection Mode Evaluation Board User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9252-3PORT. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9252-3PORT as a development tool for the Microchip LAN9252 EtherCAT® slave controller. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9252-3PORT.
- **Chapter 2. "Board Details"** – Includes details and instructions for using the EVB-LAN9252-3PORT.
- **Chapter 3. "Board Configuration"** – Describes the various EVB-LAN9252-3PORT board features, including jumpers, LEDs, test points, system connections, and switches.
- **Appendix A. "EVB-LAN9252-3PORT Evaluation Board"** – This appendix shows the EVB-LAN9252-3PORT.
- **Appendix B. "EVB-LAN9252-3PORT Evaluation Board Schematics"** – This appendix shows the EVB-LAN9252-3PORT schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9252-3PORT Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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Technical support is available through the web site at:
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DOCUMENT REVISION HISTORY

Revision A (August 2015)

- Initial Release of this Document.

Revision B (August 2015)

- Updated **Appendix C. "Bill of Materials (BOM)"**

Revision C (October 2017)

- Corrected miscellaneous grammar and typos
- Corrected details in **Section 3.2.4.3 "3 Port Mode"**
- Corrected Table 3-15 for chip_mode_strap value and description

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9252 is a 2/3 port EtherCAT® slave controller with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver.

Each port receives an EtherCAT frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards the frames to the next logical port, if there is either no link at a port, or if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT Processing Unit. The loop settings can be controlled by the EtherCAT master.

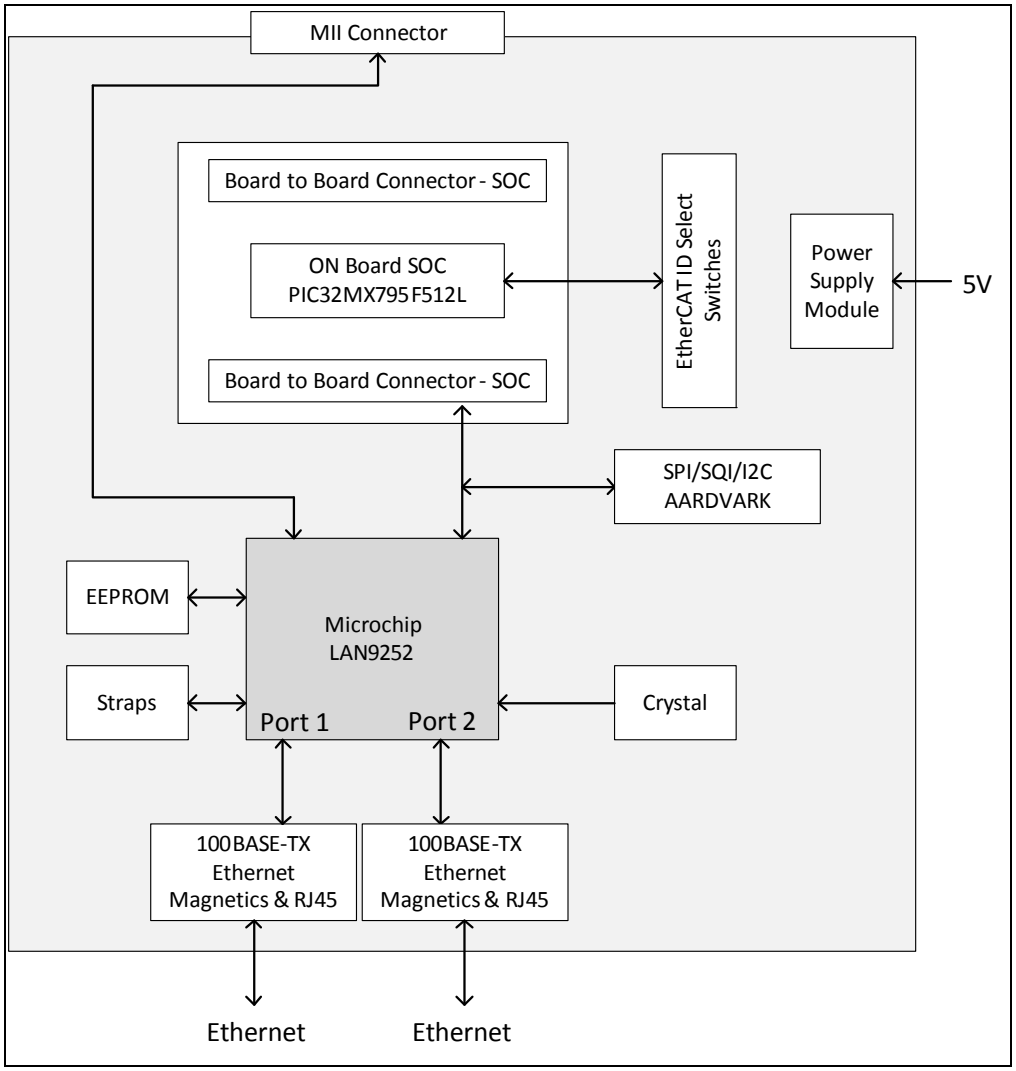
Packets are forwarded in the following order:

Port 0 -> EtherCAT Processing Unit -> Port 1 -> Port 2

The EtherCAT Processing Unit (EPU) receives, analyses and processes the EtherCAT data stream. The main purpose of the EtherCAT Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT master and from the local application. Data exchange between master and slave application is comparable to a dual-ported memory (process memory), enhanced by special functions e.g. for consistency checking (SyncManager) and data mapping (FMMU). Each FMMU performs the task of bitwise mapping of logical EtherCAT system addresses to physical addresses of the device.

The scope of this document is to describe the EVB set-up for LAN9252 which supports 3-port mode and its jumper configurations. The LAN9252 is connected to an RJ45 Ethernet jack with integrated magnetics for 100BASE-T connectivity. A simplified block diagram of the LAN9252 can be seen Figure 1-1.

FIGURE 1-1: EVB-LAN9252-3PORT BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- LAN9252 Datasheet
- AN 8.13 Suggested Magnetics
- EVB-LAN9252-3PORT Schematics

1.3 TERMS AND ABBREVIATIONS

- ESC - EtherCAT® Slave Controller
- EVB - Evaluation Board
- SPI - Serial Protocol Interface
- 100BASE-TX- 100 Mbps Fast Ethernet, IEEE802.3u Compliant
- GPIO - General Purpose I/O
- MII - Media Independent Interface
- RMII - Reduced Media Independent Interface

Chapter 2. Board Details

2.1 POWER

Power is applied through 5V DC jack J1 using an external wall power supply. Slide switch SW1 enables power to the board, providing 5V to the onboard 3.3V switching regulator. A glowing green LED (D1) indicates successful generation of 3.3V. This power is supplied to the LAN9252 and the integrated 1.2 V regulator, which supplies power to the internal core logic.

2.2 RESETS

2.2.1 Power-on Reset

A power-on reset occurs whenever power is initially applied to the LAN9252 or if the power is removed and reapplied to the LAN9252. This event resets all circuitry within the LAN9252. After initial power-on, the LAN9252 can be reset by pressing the reset switch (SW2). The reset LED D2 will assert (red) when the LAN9252 is in reset condition.

For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.2.2 Reset Out

The LAN9252 reset pin can be configured as an output to reset the SoC. The RST# pin becomes an open-drain output and is asserted for the minimum required time of 80ms

2.3 CLOCK

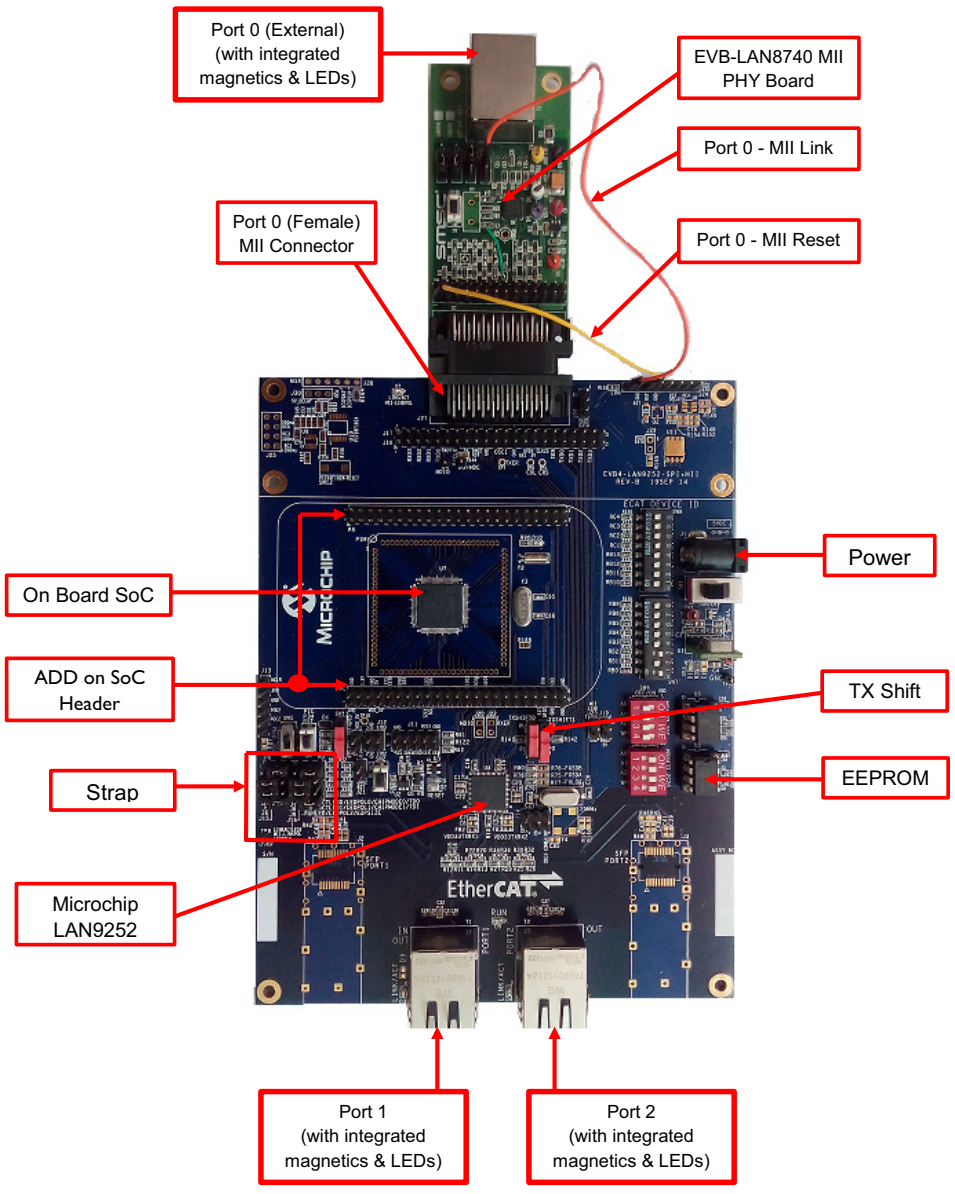
The LAN9252 requires an external 25Mhz crystal or clock.

By default, header J14 pins 1-2 are shorted to connect the 25 MHz crystal Y1 to the internal oscillator of the LAN9252.

Chapter 3. Board Configuration

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the LAN9252 in 3-port mode is shown in Figure 3-1.

FIGURE 3-1: LAN9252 - 3 PORT MODE

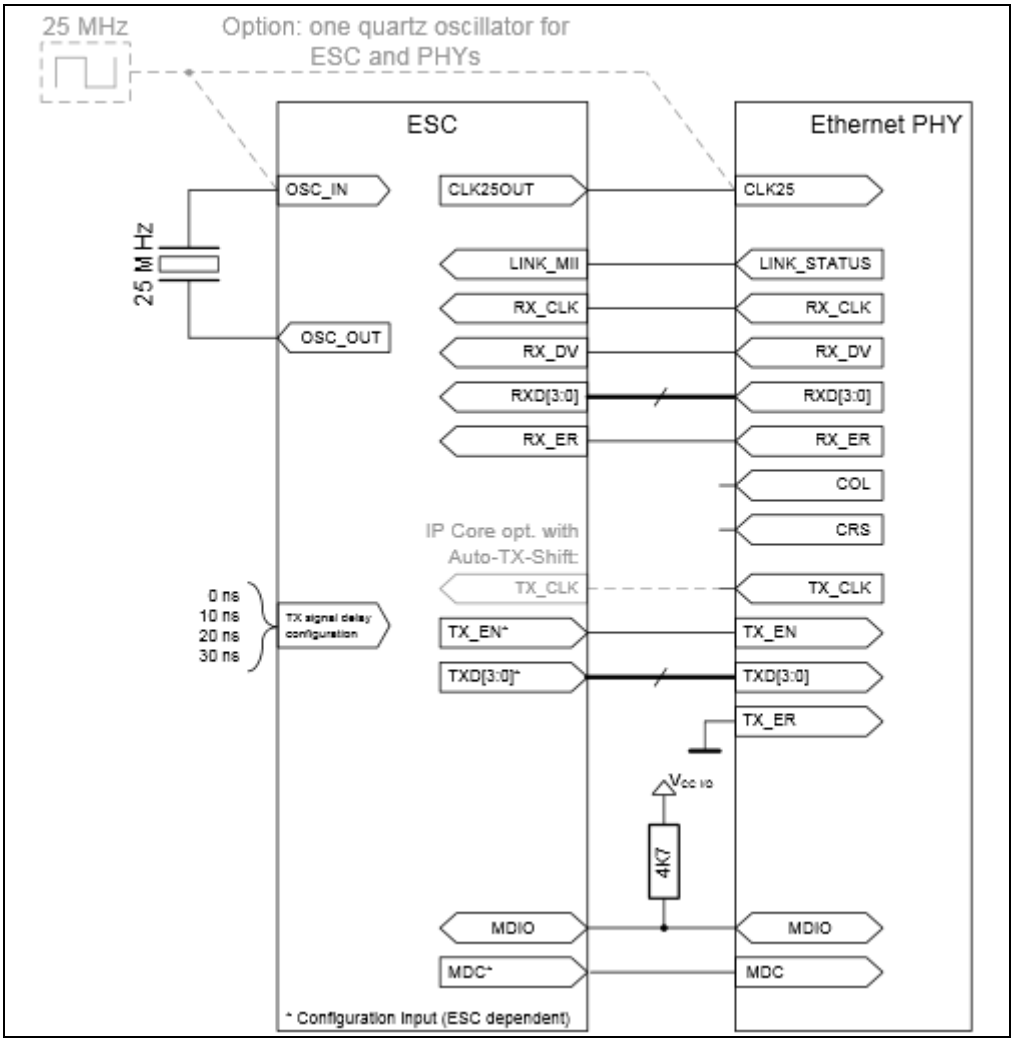


Note: 3-port Mode: Port 1 and Port 2 are both Internal, Port 0 is External.

3.1 EXTERNAL PHY CONNECTION MODE

Figure 3-2 shows the connectivity between the EtherCAT Slave Controller and PHY. The clock source of the Ethernet PHYs and ESC must be the same quartz or quartz oscillator. TX_CLK is usually not connected unless automatic TX Shift compensation is used, because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC for TX_CLK phase shift compensation. LINK_STATUS is an LED output indicating a 100 Mbit/s (Full Duplex) link.

FIGURE 3-2: EXTERNAL PHY CONNECTION



3.2 JUMPER SETTINGS

The default jumper settings for the LAN9252 are provided in Table 3-1.

TABLE 3-1: DEFAULT JUMPER SETTINGS

Jumper	Pin Settings
J4 & J7	2-3
J5 & J8	1-2
J6 & J9	1-2
J15 & J16	2-3
J19,J20,J21,J22 & J23	OPEN

3.2.1 Strap Options

The following sections describe the default settings and jumper descriptions for the EVB-LAN9252-3PORT. These defaults are the recommended configurations for evaluation of the LAN9252. These settings may be changed as needed, however, any deviation from the defaults settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

3.2.1.1 JUMPERS J4:J9 AND J15:J16

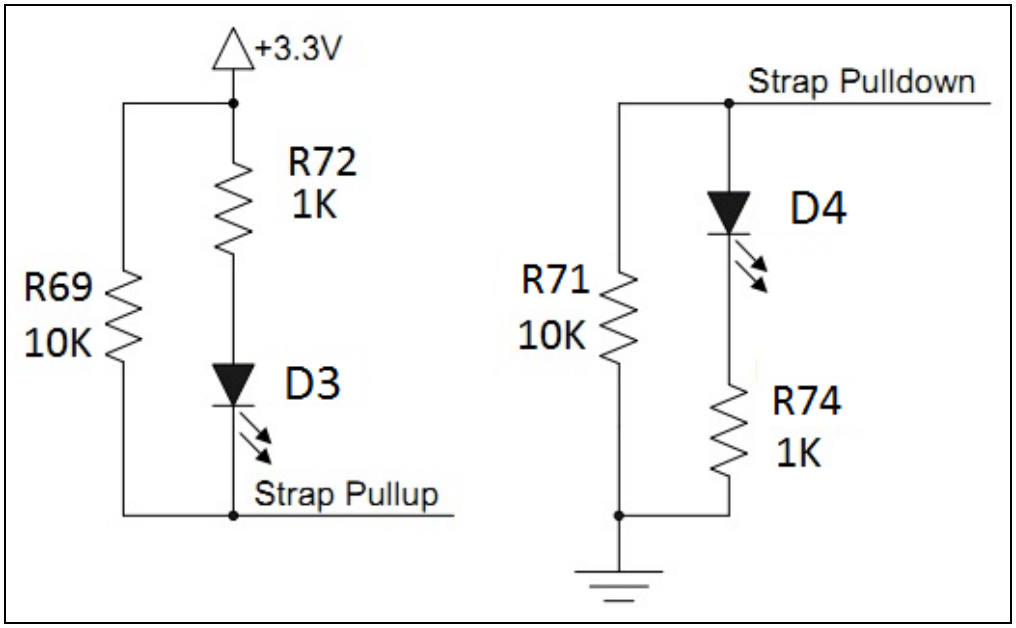
Jumpers J4 through J9 and J15 through J16 set various functions of the LAN9252. They can also be used as GPIOs or LED drivers. When used as LED drivers, as they are on the EVB-LAN9252-3PORT, they are connected a specific way to set the strap value to a "1", and another way to set the strap value to a "0". Figure 3-3 illustrates the schematic connections with the D3 circuit as a pull-up, and the D4 circuit as a pull-down. To illuminate D3, the LAN9252 will drive the cathode of the D3 low. To illuminate D4, the LAN9252 will drive the cathode of the D4 high.

The J4 - J15 jumpers must be configured in pairs to identical settings in order to realize the D3 circuit or the D4 circuit. The pairings are as follows:

- J4 & J7
- J6 & J9
- J5 & J8
- J15& J16

The following subsections detail the jumper pair settings, their associated strap settings, and the functional effects of setting the straps. All strap values are read during power-up and on the rising edge of nRST signal. Once the strap value is set, the LAN9252 will drive the LED's high or low for illumination according the strap value. For other designs which may use these pins as GPIOs, refer to the LAN9252 datasheet for additional information. In those cases, internal default straps must be changed by an I^2C or SMI master or via EEPROM fields.

FIGURE 3-3: LED STRAP CIRCUIT



3.2.1.2 EEPROM CONFIGURATION

EEPROM_size_strap (J6 & J9): This strap determines the EEPROM size range.

A low selects 1K bits (128 x 8) through 16K bits (2K x 8)_24C16.
A high selects 32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8)_24C512.

TABLE 3-2: EEPROM SIZE CONFIGURATION

Header	Pin Settings	eeprom_size_strap Value	Description
J6 & J9	1-2 (Default)	1	EEPROM size = 32K bits (4K x 8) through 4Mbits (512K x 8).
J6 & J9	2-3	0	EEPROM size = 1K bits (128 x 8) through 16K bits (2K x 8).

3.2.1.3 TX SHIFT STRAP

EtherCAT MII Port TX Timing Shift Strap is used to configure default value of the EtherCAT MII Port TX Timing Shift Strap “TX_SHIFT[1:0]”. These straps determine the value of the MII TX Timing Shift for the MII.

TABLE 3-3: ETHERCAT MII PORT TX TIMING SHIFT STRAP OPTIONS

TX_SHIFT 1	TX_SHIFT 0	TX Timing Shift (ns)
0	0	20
0	1	30 (Default)
1	0	0
1	1	10

TABLE 3-4: MII TX TIMING SHIFT CONFIGURATIONS

Switch	Short Pins	TX_SHIFT[1:0]	Switch KNOB Position
SW9	1-2	01	DOWN
SW10	1-3		UP

Note: For switch P/N: 450301014042, pin 1 is at the middle of the switch. To short 1-2, the knob position must be in the 1-3 position, and vice versa.

3.2.1.4 COPPER AND FIBER STRAPS

The LAN9252 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and SFP 100BASE-FX (Fiber) modes. By default, Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must to be configured.

Note: The vendor part number for the SFP is Finisar/FTLF1217P2

3.2.1.4.1 Copper Mode Strap

The EVB-LAN9252-3PORT is set to Copper Mode by default. Table 3-5 details the required strap resistor settings for Copper Mode operation.

TABLE 3-5: COPPER MODE STRAP RESISTORS

Resistors	Signal Names	Description
R79 (10K)	FXLOSEN	Copper twisted pair for ports A and B further determined by FXSDENA and FXSDENB
R76, R80 (10K)	FXSDA/FXSDB	Configures Port 0 and Port 1 to Copper Mode

Note: R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-6 must be assembled for Copper mode operation.

TABLE 3-6: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19,R21, R23	Port 0 Copper mode is Enabled
R31, R33, R35, R37	Port 1 Copper mode is Enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

3.2.1.4.2 Fiber Mode Strap

The EVB-LAN9252 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resisters must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (See **Section 3.2.1.4.1 "Copper Mode Strap"**).

Table 3-7 details the required strap resistor settings for Fiber Mode operation.

TABLE 3-7: FIBER MODE STRAP RESISTORS

Resistors	Description
R77 (10K)	Configures Port 0 & 1 to FX_LOS Mode
R75, R78 (10K)	Configures Port 0 & 1 to Fiber mode, respectively

Note: R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-8 must be assembled for Fiber Mode operation.

TABLE 3-8: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 0 Fiber mode Enabled
R30, R32, R34, R36	Port 1 Fiber mode Enabled

Note: R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

3.2.1.4.3 FX-LOS Fiber Mode Strap

The EVB-LAN9252-3PORT is set to Copper Mode by default. Table 3-9 details the required strap resistor settings for FX-LOS Fiber Mode operation.

TABLE 3-9: FX-LOS FIBER MODE STRAP RESISTOR SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (V)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port1
Populate	Populate	1.5	A level greater than 1.5V and below 2V selects FX-LOS for Port 0 and FX-SD / copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (DEFAULT)	A level of 0V selects FX-SD / copper twisted pair for Ports 0 and 1, further determined by FXSDA and FXSDB

Note: The above strap details describe the LAN9252 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

3.2.2 LED Indicators

LED indicators D3, D4 and D7 are used to indicate the Link/Activity status on the corresponding EVB ports, as detailed in Table 3-10. The Link/Act LED should be ON at each port when the cable is present. If the Link/Act LED is not ON, it indicates there is an issue with the connection or cable.

TABLE 3-10: D3, D4 AND D7 LINK/ACTIVITY LED STATUS INDICATORS

State	Description
Off	Link is down
Flashing Green	Link is up, with activity
Steady Green	Link is up, no activity

Additionally, the LED is used as a RUN indicator (green) to show the AL status of the EtherCAT State Machine (ESM), as detailed in Table 3-11.

TABLE 3-11: ESM AL STATUS

State	Description
Off	The device is in INITIALIZATON state
Blinking (on 200ms, off 200ms)	The device is in PRE-OPERATIONAL state
Single Flash (on 200ms, off 1000ms)	The device is in SAFE-OPERATIONAL state
On	The device is in OPERATIONAL state
Flickering (on 50ms, off 50ms)	The device is booting and has not yet entered the INITIALIZATION state, or the device is in the BOOTSTRAP state and firmware download is in progress. (Optional. Off when not implemented.)

Additionally, LED D10 is used as Error LED and the LED D9 is DNP.

3.2.3 EEPROM Switch

The EVB-LAN9252-3PORT utilizes 0x50 (7-bit) I^2C slave addressing. The SW3 switch can be used to select the A0, A1, and A2 address bits, as shown in Figure 3-4 and Table 3-12. The eighth bit of the slave address determines if the master device wants to read or write to the EEPROM (24FC512).

FIGURE 3-4: SLAVE ADDRESS ALLOCATION

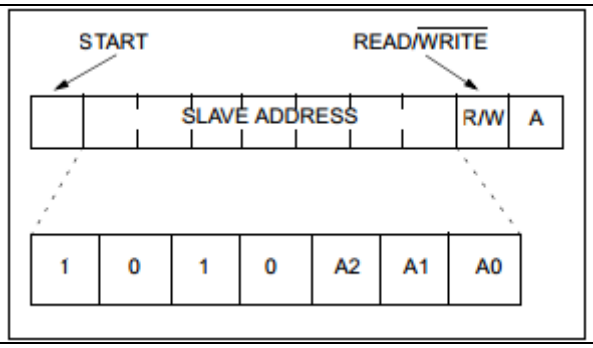


TABLE 3-12: EEPROM SWITCH

Ref. Des	Description	Settings
SW3	I^2C EEPROM Address selection (A0,A1,A2) see Figure 3-4	ON for logic 0 (default) OFF for logic 1

3.2.4 SPI + 3 Port Mode Selection

3.2.4.1 SPI

The SPI lines are directly connected to the SOC. No jumper settings are required for SPI.

3.2.4.2 SPI/SQI/I^2C AARDVARK®

J11 & J12 connectors are used for Aardvark/SPI headers. Respective pin details are given below in Table 3-13. Resisters R61, R62 & R122 must be populated to use this option. By default, R61, R62 & R122 are DNP.

TABLE 3-13: SPI/SQI/I^2C AARDVARK® PIN DETAILS

Signal	Pin No
SCL	J11.1
SDA	J11.3
SCK	J11.7
SCS#	J11.9
SI(SIO0)	J11.8
SO(SIO1)	J11.5
SIO2	J12.3
SIO3	J12.4

3.2.4.3 3 PORT MODE

The following Assembly/jumper settings are used to configure LAN9252 into 3-Port mode.

3.2.4.3.1 Assembly of the Boards

The MII Female Connector (J27) is used to connect the External PHY Board. The EVB-LAN8740 MII PHY Board has been used as the External PHY Board as shown in Figure 3-2.

3.2.4.3.2 External PHY - Power

The Jumper (J26) is used to supply “on-board 5V or delayed 5V” to the external PHY Board.

TABLE 3-14: EXTERNAL PHY BOARD PIN SETTINGS

Header	Pin Settings	Description
J26	1-2	Connects on-board 5V to an external PHY Board (Default)
J26	2-3	Connects Delayed 5V to an external PHY Board in Enhanced Link detection

3.2.4.3.3 External PHY - MII Link connection

Connect Pin 1 of J24 (on EVB-LAN9252-3Port) to pin 2 of JP4 (on EVB-LAN8740) through jumpers as shown in Figure 3-2.

Also, make sure JP1 and JP2 (on EVB-LAN8740) are in the 1-2 position, and JP3 (on the EVB-LAN8740) is in the 2-3 position.

3.2.4.3.4 External PHY - MII Reset connection

Connect Pin 3 of J24 (on EVB-LAN9252-3Port) to pin 1 of J1 (on EVB-LAN8740) through jumpers as shown in Figure 3-2.

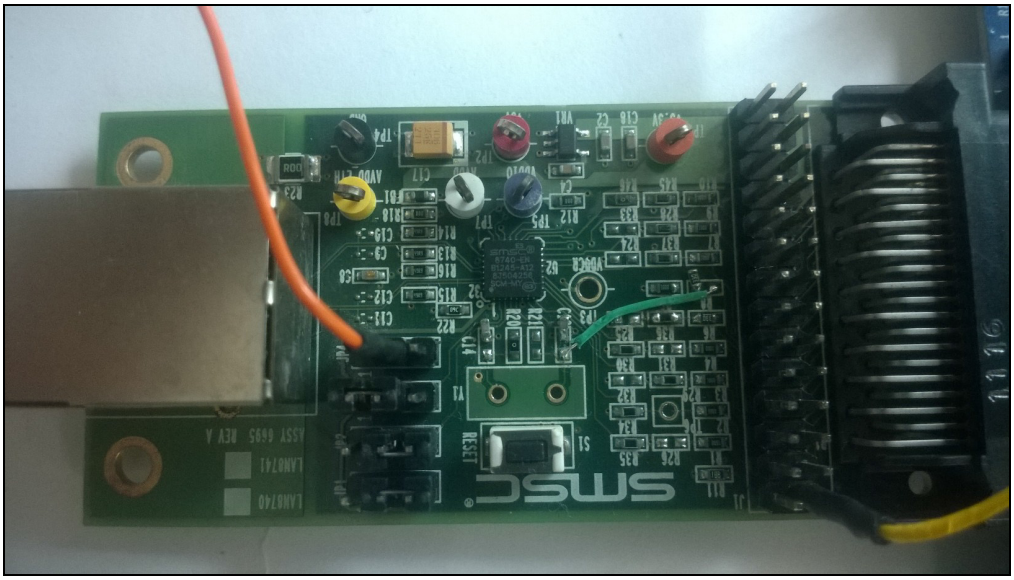
3.2.4.3.5 External PHY - CLK

The MII_CLK25 from the LAN9252 is available on J27-12th pin. When MII connection is made with the external PHY board, this signal is routed to the Master Clock of the External PHY.

Note: The EVB-LAN8740 is used for an External PHY. Refer to http://ww1.microchip.com/downloads/en/DeviceDoc/evb8740_user.pdf for more details on the EVB-LAN8740.

Remove on board crystal Y1, C13 (capacitor near Y1), and resistor R8. Connect the connector side end of R8 to the LAN8740 OSCO pin (which is pin 1 of Y1 on the EVB-LAN8740) as shown below in Figure 3-5 (green wire). This will connect MII-CLK25 from the MII connector to the external LAN8740 PHY.

FIGURE 3-5: EVB-LAN8740



3.2.4.3.6 Chip Mode Selection

Chip Mode Straps (J4,J7 & J5,J8) are used configure the default value of the EtherCAT Chip Mode Strap "chip_mode_strap[1:0]". This strap determines the number of active ports and port types.

TABLE 3-15: CHIP MODE CONFIGURATION

Header	Pin Settings	chip_mode_strap[1:0]	Description
J4,J7	2-3	10b	3-port downstream mode. Ports 0 and 1 are connected to internal PHYs A and B. Port 2 is connected to the external MII pins.
J5,J8	1-2		

Note: The default setting of the EVB is chip mode 10 (3port downstream mode). Chip modes 00 and 11 are not supported by this EVB.

3.2.5 SoC

The EVB-LAN9252 supports both an on-board SoC and add-on SoC. By default, the on-board SoC is enabled. However, an external add-on SoC can be connected via the add-on SoC headers P8 and P9. The SoC selection is configured via the SW5 switch, as detailed in the following subsections.

3.2.5.1 SOC SELECTION

Whenever the ADD ON PCB is used for SoC, the Switch knob position must be UP.

The SW5 switch selects the enabled SoC. The SW5 switch knob position must be down (Text = "PIC") to select the on-board PIC. If the switch knob position is up (Text = "PIM"), then the add-on board/SoC is selected and the on-board PIC is always in the reset state. Whenever an add-on board/SoC is used, the switch knob must be in the up position.

TABLE 3-16: SOC SWITCH CONFIGURATION

Switch	Position	Settings
SW5	DOWN	PIC enabled
SW5	UP	ADD ON BOARD enabled

3.2.5.2 ON-BOARD PIC

By default, the on-board Microchip PIC32MX795F512L (U7) is used as the default SoC. The LAN9252 can be connected to the PIC using SPI interface. No jumper settings are required to establish SPI communications between PIC and LAN9252.

3.2.5.3 RESET

SW5 is used to reset the on-board PIC. The LAN9252 can also reset the SoC if the reset pin is configured to output mode. For stability, a delay of approximately 180ms is added from the 3.3V o/p to reset release.

3.2.5.4 ICSP HEADER

The programing is done using the ICSP header J13. Table 3-17 shows the PIN details of J13.

TABLE 3-17: J13 PIN DETAILS

J13 PIN No	Signals Detail
1	MLCR
2	3V3
3	GND
4	PGD2
5	PGC2
6	NC

3.2.5.5 SOC EEPROM

The EVB-LAN9252 provides an optional SoC EEPROM. Some SoCs may require an EEPROM. However, the PIC on-board SoC and PIC based add-on SoC boards do not require this EEPROM.

3.2.5.6 ADD-ON SOC

An add-on board can be attached to the EVB-LAN9252 to use an add-on SoC. The add-on board must be mounted to the P8 and P9 connectors (2x23, 100mil normal gold plated berg stick). The SW5 switch must be in the up position when using an add-on SoC. Additionally, the J10 2-pin jumper must be shorted to route power to the add-on board from the EVB-LAN9252.

An add-on board can be used for a SoC. When using an add-on board, it must be mounted at the connectors P8 & P9 (2X23, 100mil normal gold platted berg stick). The SW5 switch knob position must be UP to use this option. Also the J10 2-pin jumper must be shorted to provide power to the add-on board.

3.2.5.7 ESC ID SELECT

The signals shown in Table 3-18 are provided as EtherCAT ID selection for complex ESCs. Switches SW7, SW8 and respective pull-up resistors are used to configure the ID select signals high or low. By default, the EtherCAT ID values is set to 5. To achieve this, ID0 and ID2 are high via pull-up resistors, while the remainder of the ID select signals are low (ID1, ID3-ID15). When required, setting the respective switch knob to the on position will change the ID select signal to low.

TABLE 3-18: ID SELECT SIGNALS

ID Selection Signal	PIC PIN No	SW PIN No	Res Ref. Des
ID_SELECT_RB0	25	SW7.1	R123
ID_SELECT_RB1	24	SW7.2	R124
ID_SELECT_RB2	23	SW7.3	R126
ID_SELECT_RB3	22	SW7.4	R125
ID_SELECT_RB4	21	SW7.5	R127
ID_SELECT_RB5	20	SW7.6	R128
ID_SELECT_RB8	32	SW7.7	R129
ID_SELECT_RB9	33	SW7.8	R130
ID_SELECT_RB10	34	SW8.1	R131
ID_SELECT_RB11	35	SW8.2	R133
ID_SELECT_RB12	41	SW8.3	R134

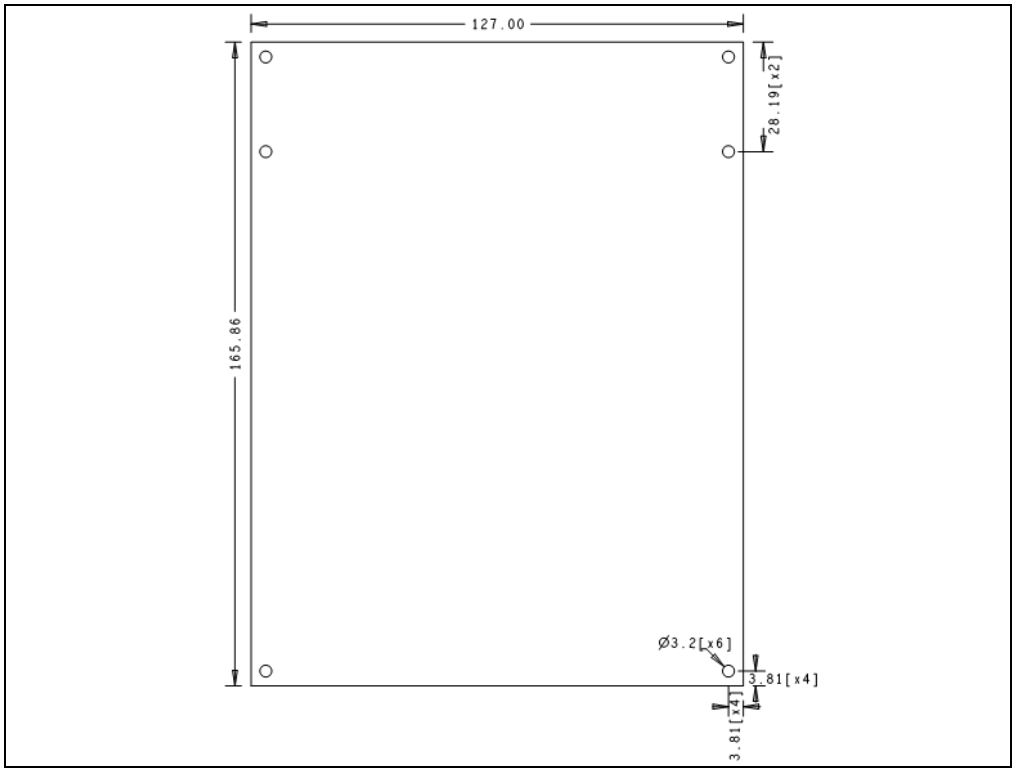
TABLE 3-18: ID SELECT SIGNALS (CONTINUED)

ID Selection Signal	PIC PIN No	SW PIN No	Res Ref. Des
ID_SELECT_RB13	42	SW8.4	R132
ID_SELECT_RC1	6	SW8.5	R135
ID_SELECT_RC2	7	SW8.6	R136
ID_SELECT_RC3	8	SW8.7	R137
ID_SELECT_RC4	9	SW8.8	R138

3.3 MECHANICALS

Figure 3-6 details EVB-LAN9252(SPI + 3 Port) mechanical dimensions. Dimensions are in mm.

FIGURE 3-6: EVB-LAN9252 MECHANICAL DIMENSIONS

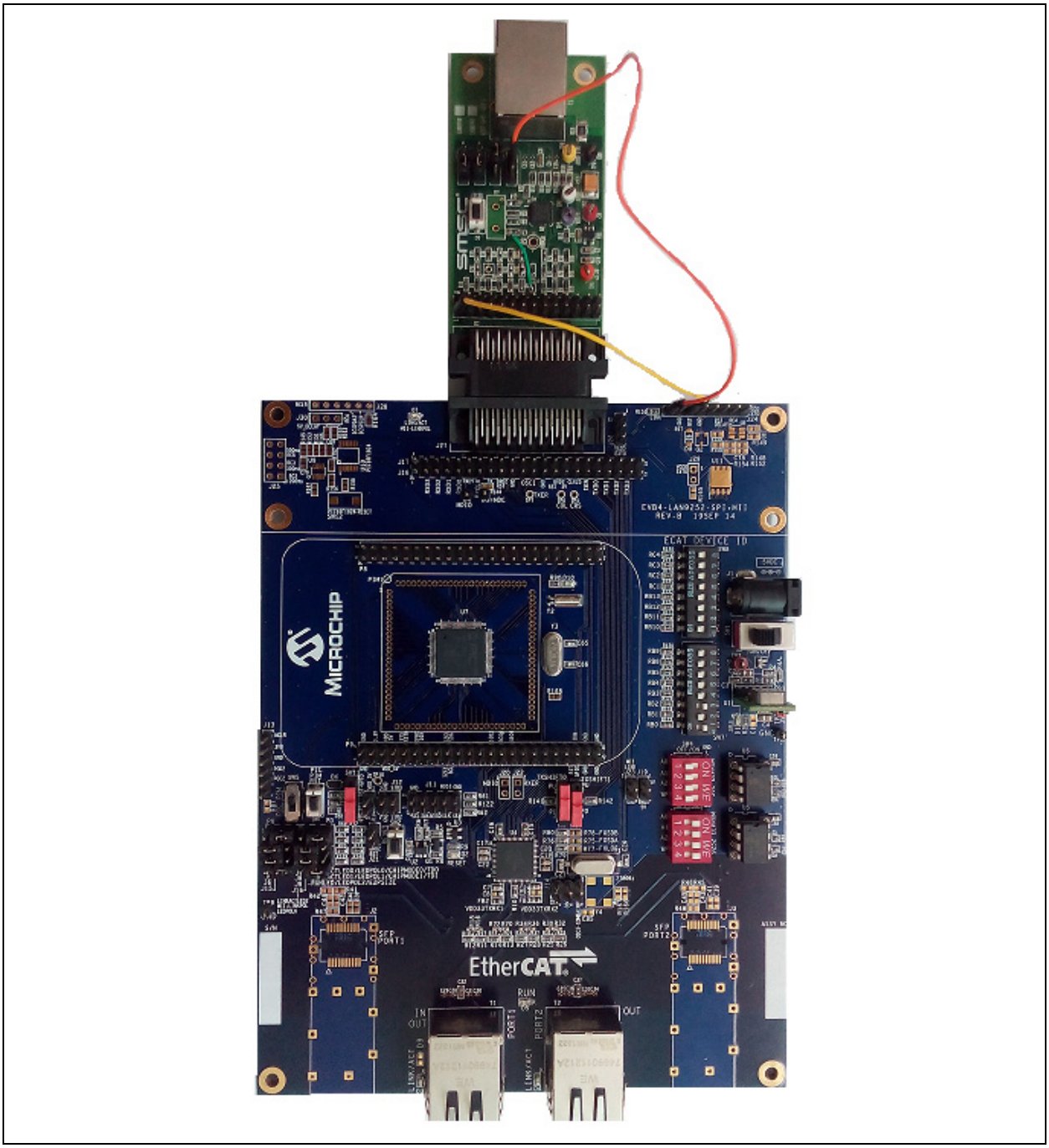


Appendix A. EVB-LAN9252-3PORT Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN9252-3PORT Evaluation Board.

FIGURE A-1: EVB-LAN9252-3PORT EVALUATION BOARD



NOTES:

Appendix B. EVB-LAN9252-3PORT Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9252-3PORT Evaluation Board Schematics.

FIGURE B-1: BLOCK DIAGRAM

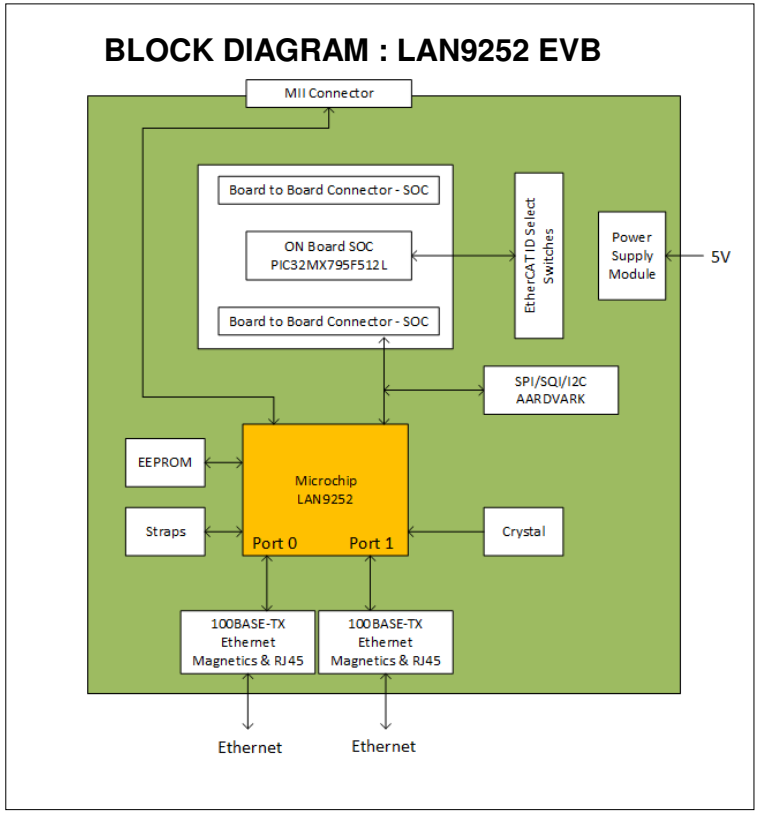


FIGURE B-2: POWER SUPPLY & RST

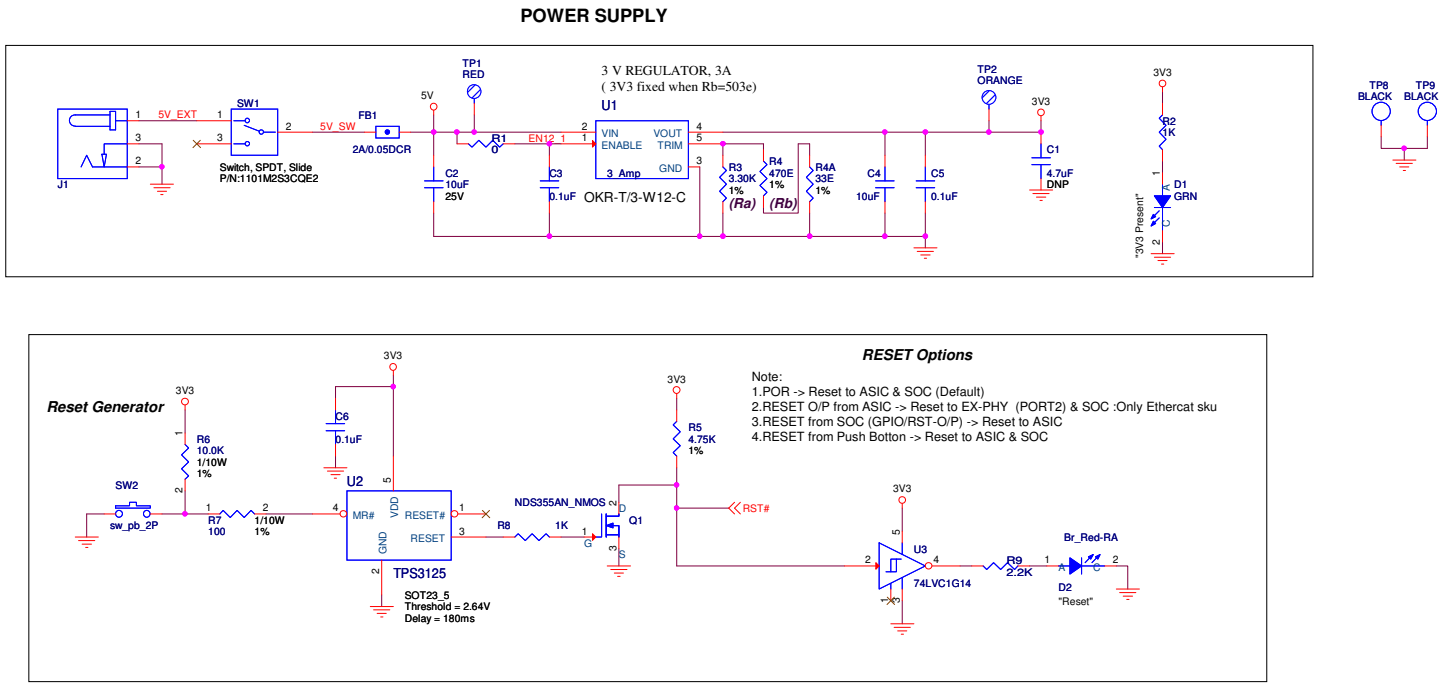


FIGURE B-3: LAN9252

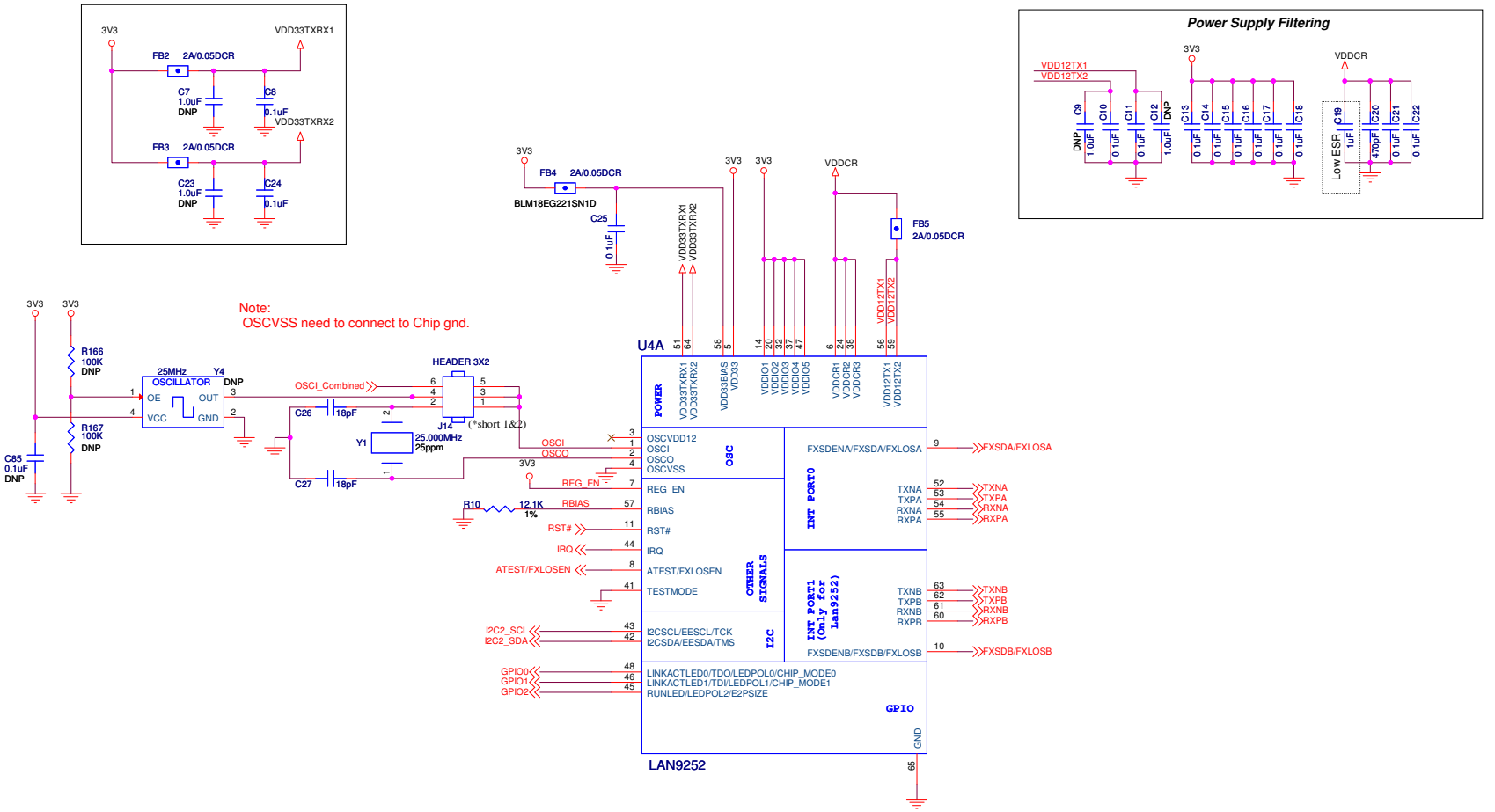


FIGURE B-4: COPPER MODE INTERFACE

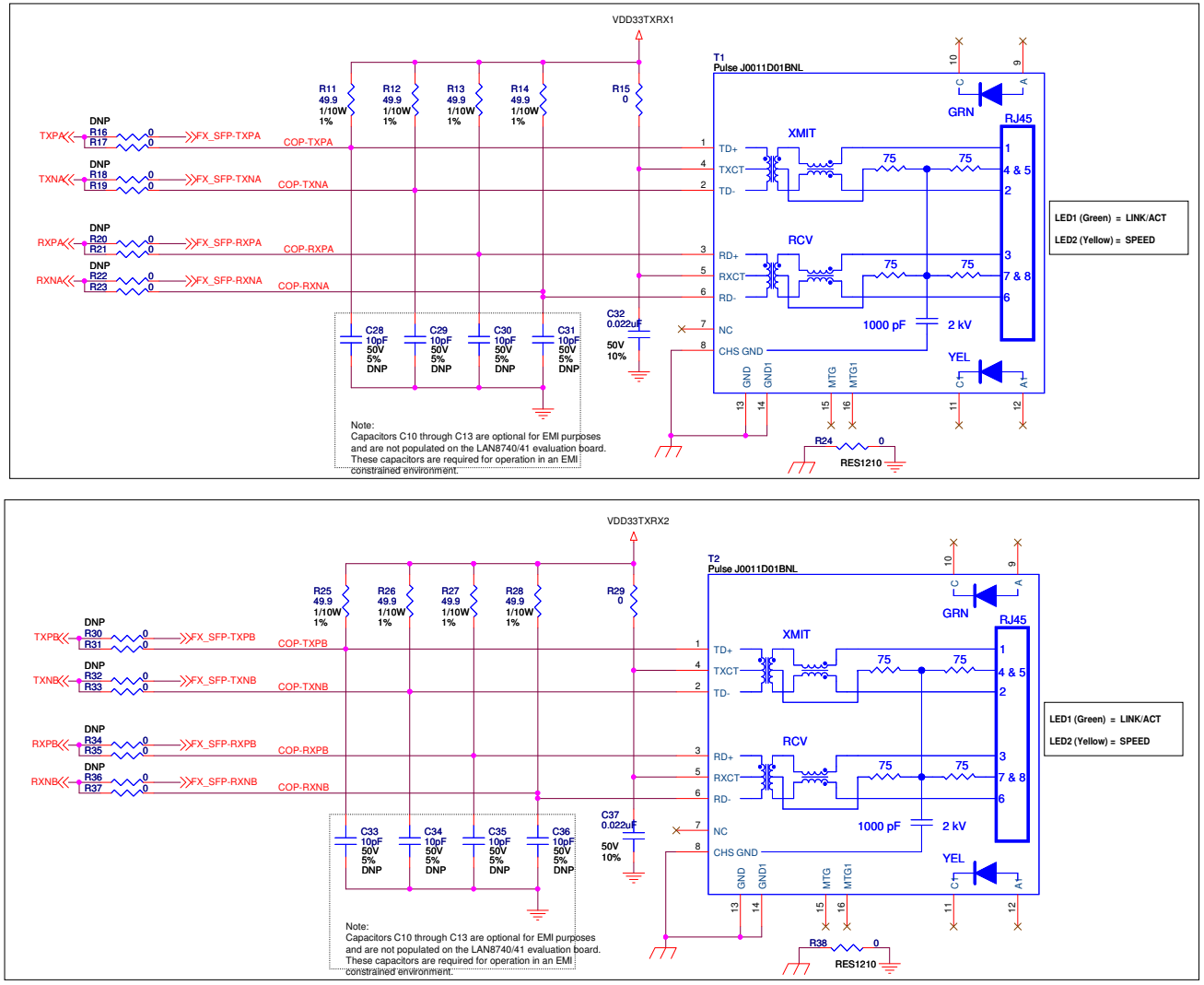


FIGURE B-5: SFP INTERFACE

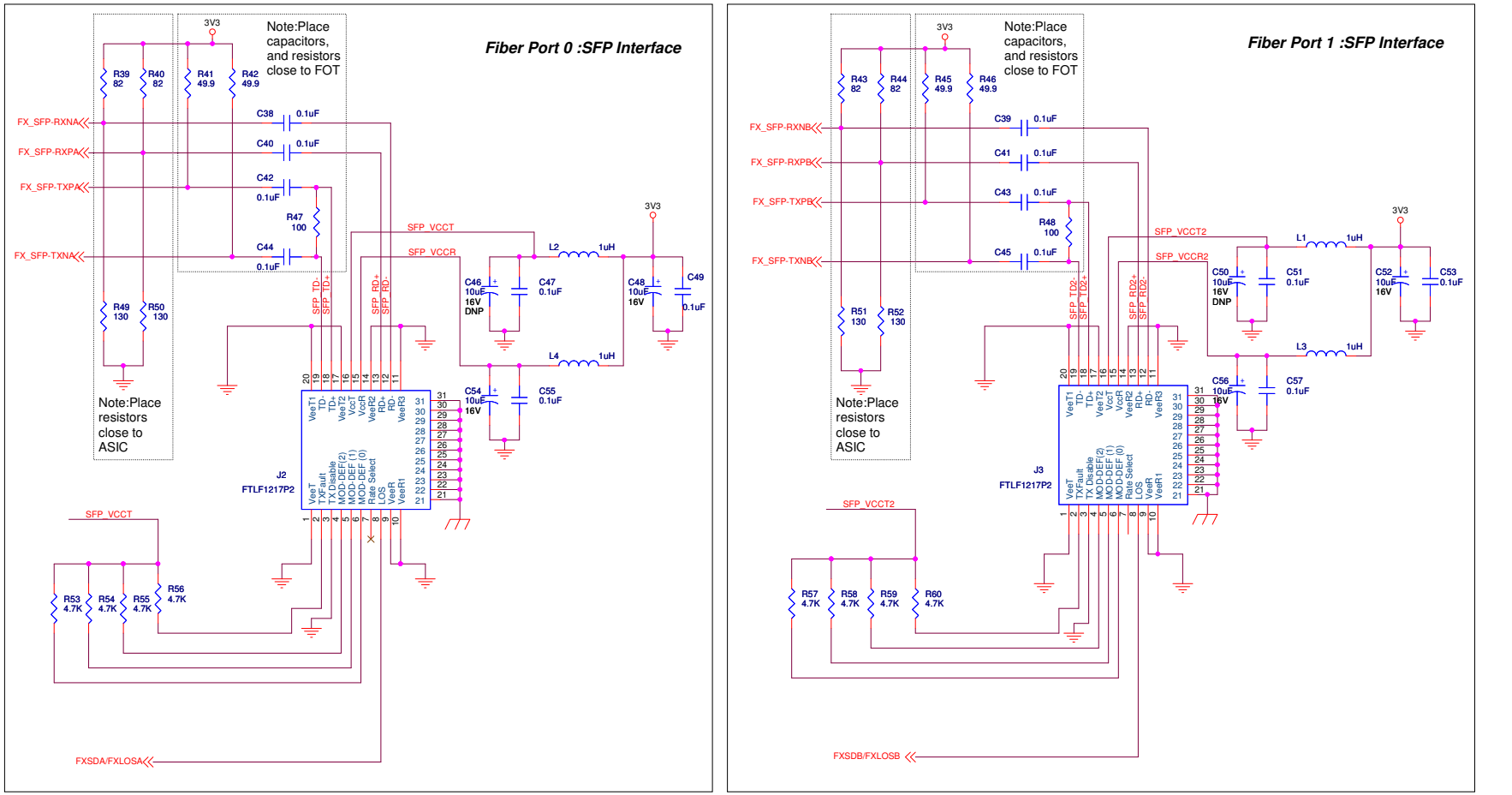
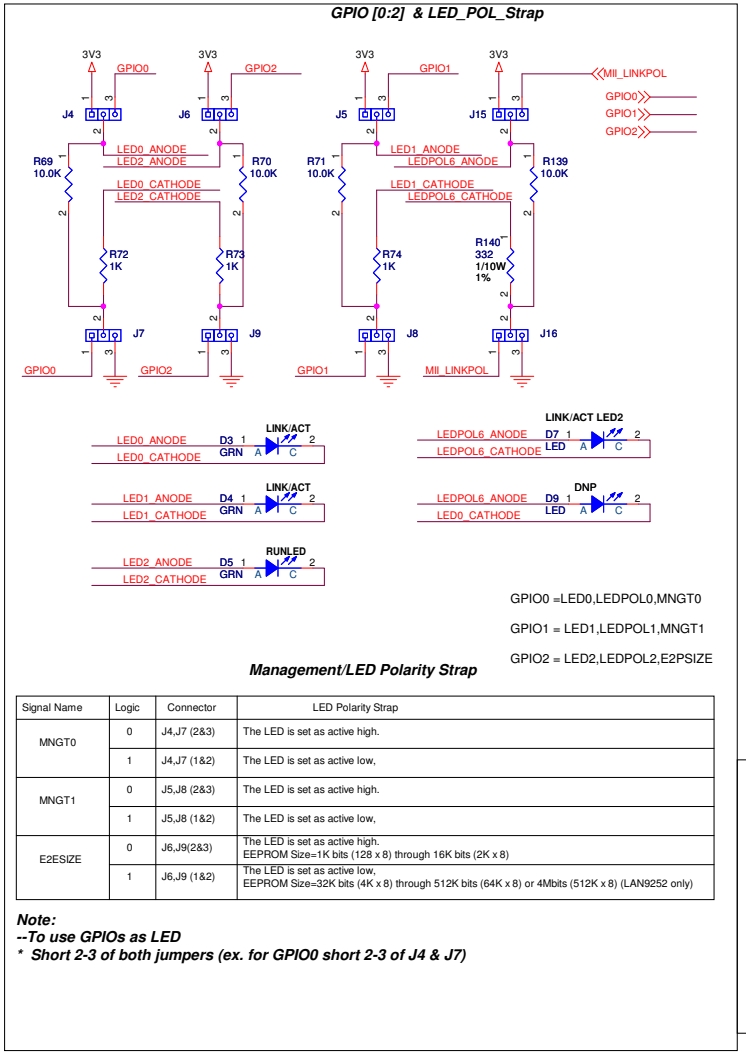


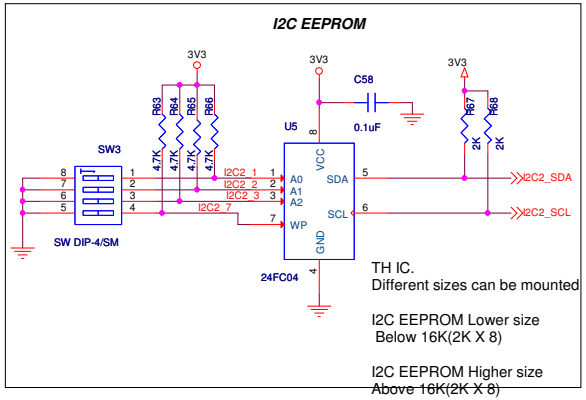
FIGURE B-6: STRAP, GPIO, I²C & FXLOS

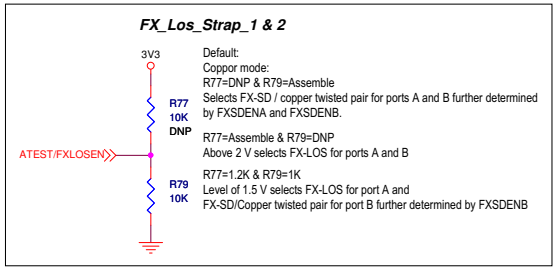


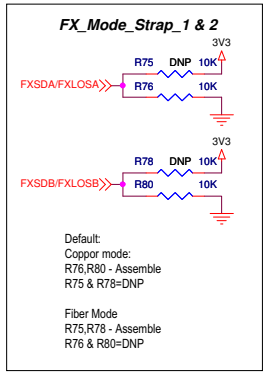
Management/LED Polarity Strap

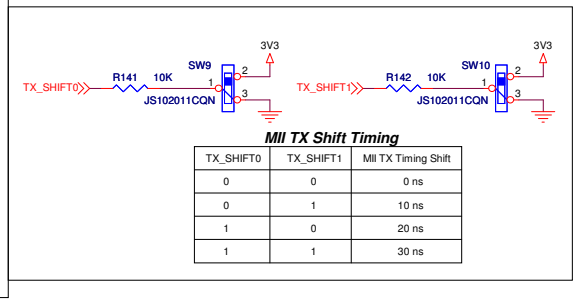
Signal Name	Logic	Connector	LED Polarity Strap
MNGT0	0	J4,J7 (2&3)	The LED is set as active high.
	1	J4,J7 (1&2)	The LED is set as active low,
MNGT1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
E2ESIZE	0	J6,J9(2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)

Note:
--To use GPIOs as LED
**** Short 2-3 of both jumpers (ex. for GPIO0 short 2-3 of J4 & J7)***





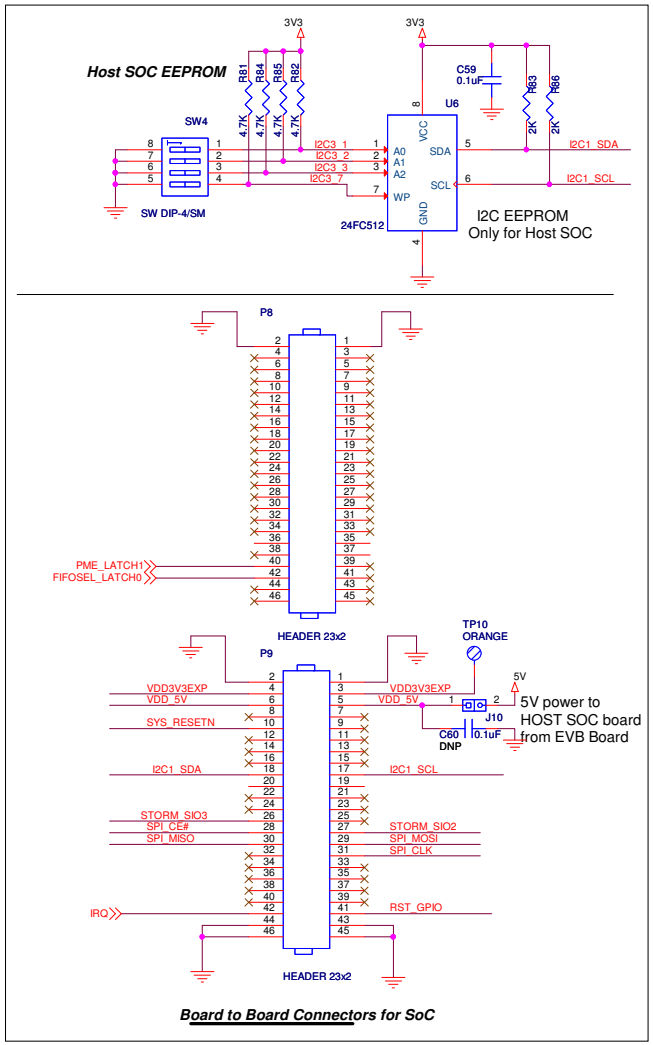


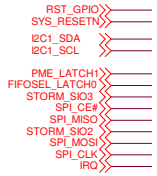


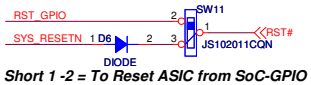
MII TX Shift Timing

TX_SHIFT0	TX_SHIFT1	MII TX Timing Shift
0	0	0 ns
0	1	10 ns
1	0	20 ns
1	1	30 ns

FIGURE B-7: B2B INTERFACE







Short 1 -2 = To Reset ASIC from SoC-GPIO
Short 2-3 = To Reset SoC from ASIC

FIGURE B-8: PIM+ON-BOARD-PIC32MX

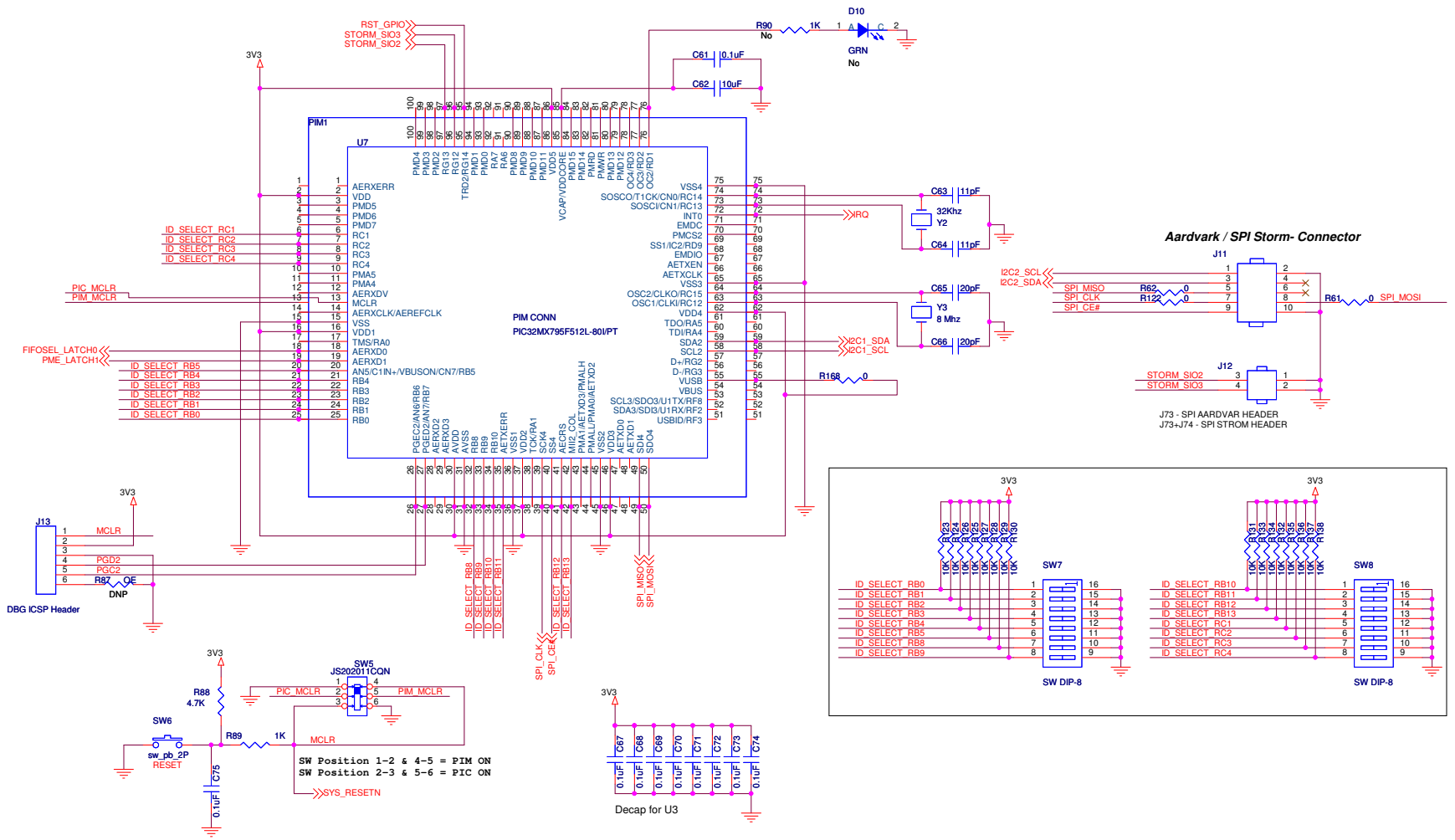
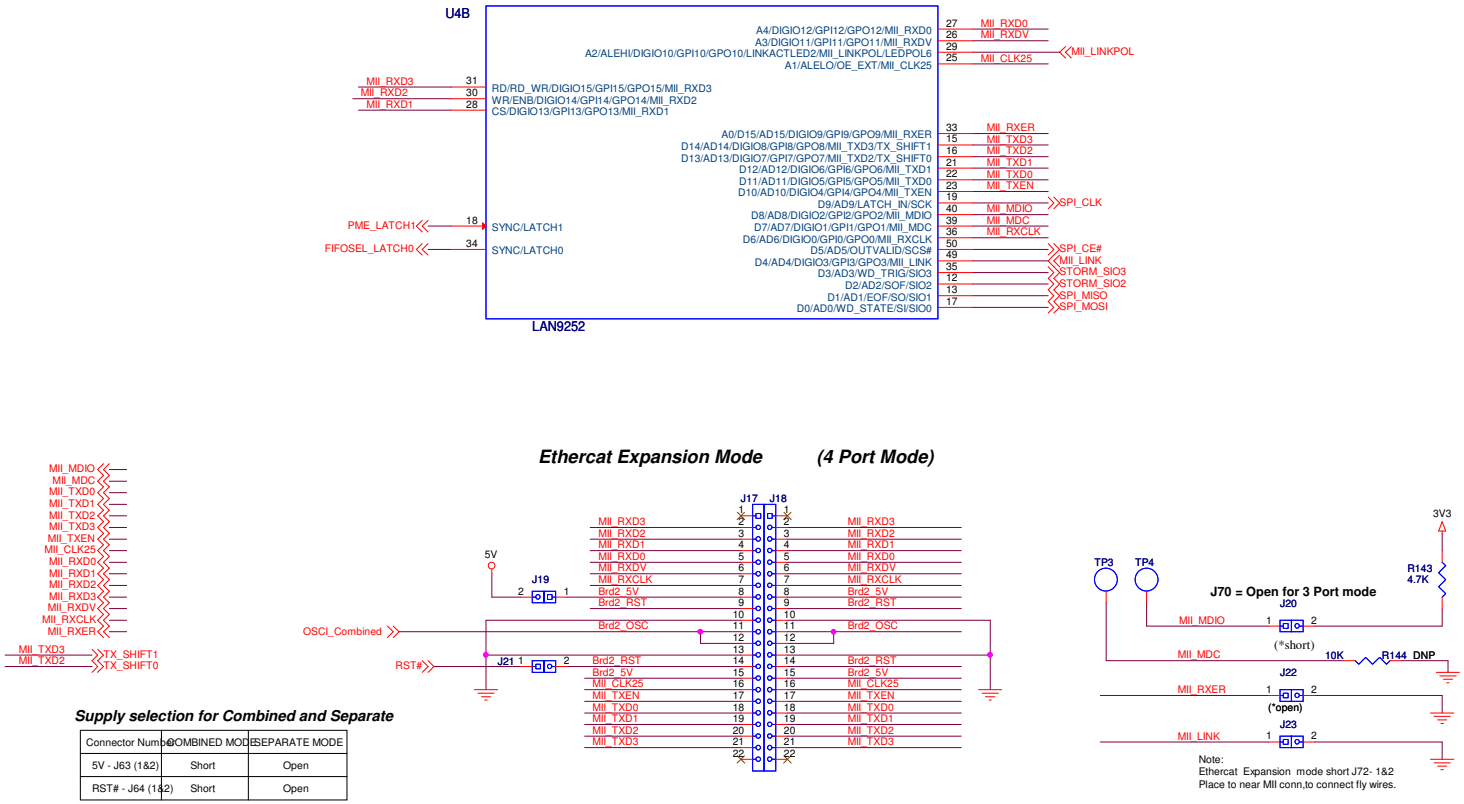


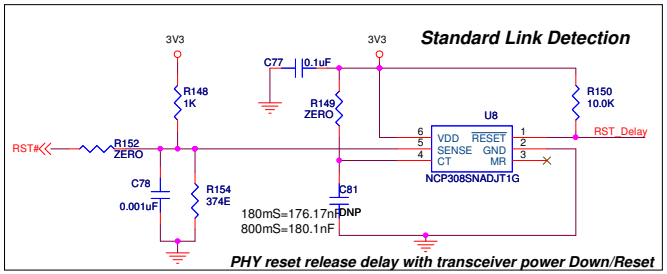
FIGURE B-9: EXPANSION MODE INTERFACE

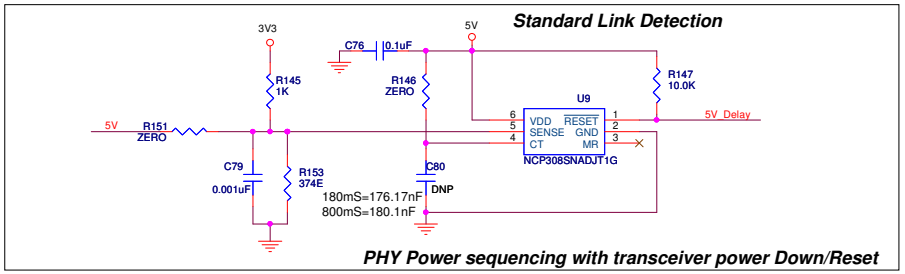


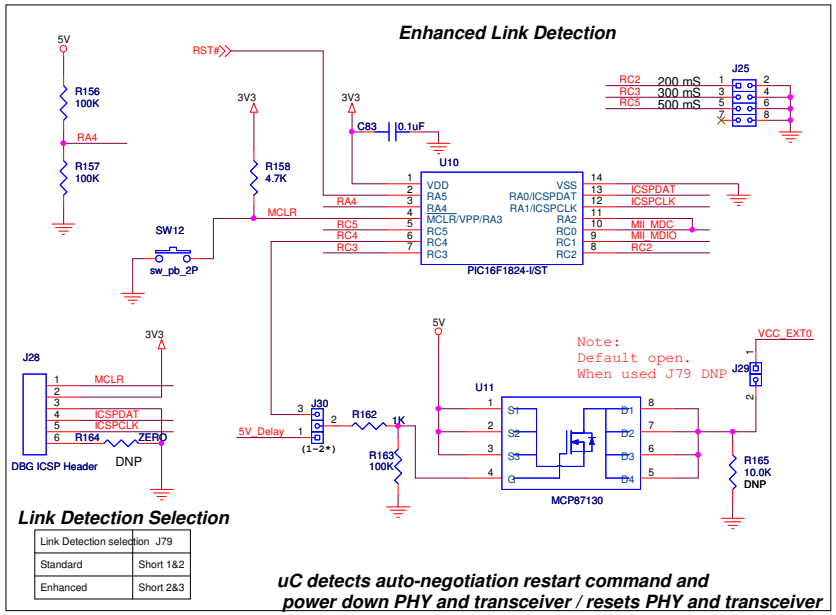
Supply selection for Combined and Separate

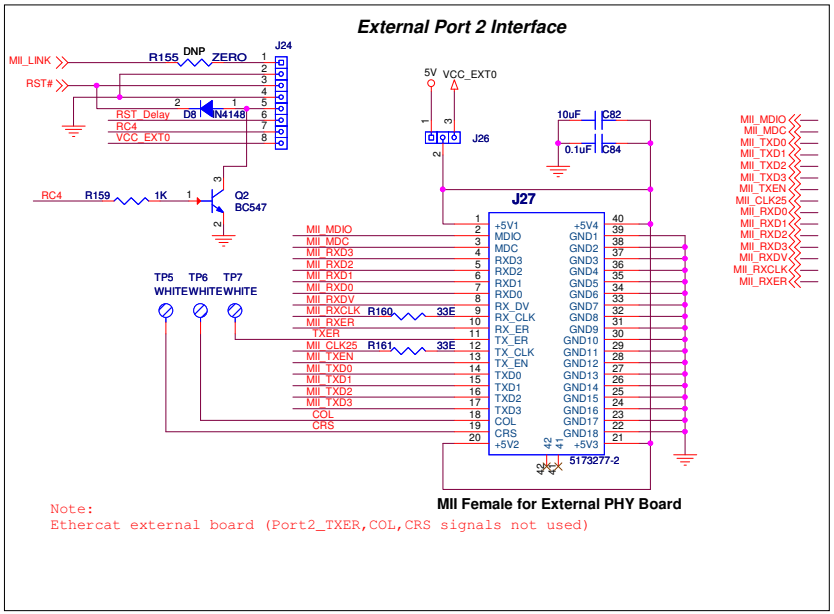
Connector Number	COMBINED MODE	SEPARATE MODE
5V - J63 (1&2)	Short	Open
RST# - J64 (1&2)	Short	Open

FIGURE B-10: ENHANCED LINK DETECTION









NOTES:

Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9252-3PORT Evaluation Board Bill of Materials (BOM).

TABLE C-1: EVB-LAN9252-3PORT EVALUATION BOARD BILL OF MATERIALS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
2	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
3	29	C3,C5,C6,C8,C10,C11,C13,C14,C15, C16,C17,C18,C21,C22,C24,C25,C58, C59,C61,C67,C68,C69,C70,C71,C72, C73,C74,C75,C84	0.1uF	CAP0603	No	Murata	GRM188R71E104KA01D
5	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
6	1	C20	470pF	CAP0603	No	Murata	GRM033R71E471KA01D
7	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
9	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
12	2	C62,C82	10uF	CAP0603	No	TDK	C1608X5R0J106K080AB
13	2	C63,C64	11pF	CAP0603	No	Murata	GRM1885C1H110JA01D
14	2	C65,C66	20pF	CAP0603	No	Murata	GRM1885C1H200JA01D
17	5	D1,D3,D4,D5,D10	GRN	LED0603	No	Stanley Electric	BG1111C-TR
18	1	D2	Br_Red-RA	LED0603	No	Stanley Electric	FR1113F
19	1	D6	DIODE	SOD123	No	Micro Commercial Co	1N4148W-TP
20	1	D7	LED	LED0603	No	Stanley Electric	BG1111C-TR
22	5	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
23	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
25	9	J4,J5,J6,J7,J8,J9,J15,J16,J26	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
26	1	J11	HEADER 5X2	TH_CONN_2X5P	No	FCI	67997-210HLF
27	1	J12	HEADER 2X2	TH_CONN_2X2P	No	FCI	67997-204HLF
28	1	J13	DBG ICSP Header	TH_CONN_1x6P	No	FCI	68000-106HLF
29	1	J14	HEADER 3X2	TH_CONN_2X2P	No	FCI	67997-206HLF
31	1	J10	HDR_1x2	TH_CONN_1X2P	No	FCI	68000-102HLF
33	1	J24	CONN_8P	TH_CONN_1X8P	No	FCI	68000-108HLF
35	1	J27	5173277-2	TH_CONN_TE-5173277_40P	No	TE	5173277-2-ND
38	2	P8,P9	HEADER 23x2	TH_CONN_2X23P	No	FCI	67997-246HLF
39	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN
41	7	R1,R15,R29,R61,R62,R122,R155	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V
42	7	R2,R8,R72,R73,R74,R89,r90	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V
43	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
44	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF

TABLE C-1: EVB-LAN9252-3PORT EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
45	3	R4A,R160,R161	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF
46	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
47	5	R6,R69,R70,R71,R139	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
48	1	R7	100E	RES0603	No	Panasonic	ERJ-3EKF1000V
49	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
50	1	R10	12.1K	RES0603	No	Rohm	CR03ERTF1212
51	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9	RES0603	No	Yageo America	9C06031A49R9FKHFT
54	8	R17,R19,R21,R23,R31,R33,R35,R37	0E	RES0402	No	Panasonic	ERJ-2GE0R00X
55	2	R24,R38	0E	RES1210	No	Vishay	CRCW12100000Z0EA
61	10	R63,R64,R65,R66,R81,R82,R84,R85, R88,R143	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
62	4	R67,R68,R83,R86	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
64	21	R76,R79,R80,R123,R124,R125,R126, R127,R128,R129,R130,R131,R132, R133,R134,R135,R136,R137,R138, R141,R142	10K	RES0603	No	Panasonic	ERJ-3GEYJ103V
66	1	R140	332	RES0603	No	Panasonic	ERJ-3EKF3320V
73	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2
74	2	SW2,SW6	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K
75	2	SW3,SW4	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904
76	1	SW5	JS202011CQN	TH_SW_DPDT_6P	No	C&K	401-2001-ND
77	2	SW7,SW8	SW DIP-8	SW_DIP_SMT_8P-ADE08S04	No	TE	1-1825058-9/ade08s04
78	3	SW9,SW10,SW11	450301014042	TH_SW_SPST_3P_10x2p5	No	Wurth electronics	450301014042
79	1	TP1	RED	TH_TP_60D40	No	Keystone	5005
80	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
	2	TP8,TP9	TEST POINT	TH_TP_60D40	No	Keystone	5001
83	2	T1,T2	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	553-1483-ND
84	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
85	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
86	1	U3	74LVC1G14	SOT23_5	No	TI	SN74LVC1G14DCKR
87	1	U4	LAN9252	IC_QFN64	No	Microchip	LAN9252
88	1	U5	24FC04	IC_DIP8_300	No	Microchip	24AA04
89	1	U6	24FC512	IC_DIP8_300	No	Microchip	24FC512-IP

TABLE C-1: EVB-LAN9252-3PORT EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
90	1	U7	PIC32MX795F512L-80I/PT	IC_TQFP100_12x12x1-0p4mm	No	Microchip	PIC32MX-795F512L-80I/PT-ND
94	1	Y1	Citizen America	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D 18-F
95	1	Y2	32Khz	TH_XTAL_ECS-31X_32KHZ	No	ECS INC	XC1392-ND
96	1	Y3	8 Mhz	th_hc49us_2p	No	Citizen Finetech	300-6017-ND

TABLE C-2: DNP COMPONENTS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
15	2	C78,C79	0.001uF	CAP0603	DNP	Murata	GRM188R71H102KA01D
3	3	C76,C77,C83	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
71	3	R156,R157,R163	100K	RES0603	DNP	Panasonic	ERJ-3EKF1003V
42	4	R145,R148,R159,R162	1K	RES0603	DNP	Panasonic	ERJ-3GEYJ102V
34	1	J25	2x4	Th_CONN_2X4P	DNP		
69	2	R153,R154	374E	RES0603	DNP	Panasonic	ERJ-3EKF3740V
61	1	R158	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
40	1	Q2	BC547	SOT23	DNP	Diodes Incorporated	MMBT4401-7-F
31	4	J29,J19,J21,J23	CONN_2P	TH_CONN_1X2P	DNP		
30	2	J17,J18	1x22	TH_CONN_1X22P	No	FCI	68000-122HLF
28	1	J28	DBG ICSP Header	TH_CONN_1x6P	DNP		
25	1	J30	HDR_1x3	TH_CONN_1X3P	DNP		
21	1	D8	IN4148	SOD123	DNP	Micro Commercial Co	1N4148W-TP
93	1	U11	MCP87130	IC_PDFN8_5x6mm_MCP8713	DNP	Microchip	MCP87130T-U/LCTR-ND
91	2	U8,U9	NCP308SNADJT1G	SOT23_6	DNP	ON Semiconductor	NCP308SNADJT1G-ND
92	1	U10	PIC16F1824-I/ST	IC_TSSOP14-4P5X5MM	DNP	Microchip	PIC16F1824-I/ST-ND
82	3	TP5,TP6,TP7	WHITE	TH_TP_60D40	DNP	Keystone	5002
31	1	J20	CONN_2P	TH_CONN_1X2P	DNP		
32	1	J22	CONN_2P	th_conn_1x2p	DNP		
74	1	SW12	sw_pb_2P	sw_pb_2P	DNP	Panasonic	EVQ-PJU04K
1	1	C1	4.7uF	CAP0603	DNP	Murata	GRM188R60J475KE19D
4	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP	Murata	GRM188R61C105KA93D
8	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP	Murata	GRM188R61C105KA93D

TABLE C-2: DNP COMPONENTS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
10	14	C38,C39,C40,C41,C42,C43,C44,C45, C47,C49,C51,C53,C55,C57	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
11	6	C46,C48,C50,C52,C54,C56	10uF	CAP_B_3528	DNP	Kemet	B45190E3106K209
16	2	C80,C81	TBD	CAP0603	DNP		
24	2	J2,J3	FTLF1217P2	CONN_FX_SFP_FTLF1217P2	DNP	Finisar	775-1011-ND
36	4	L1,L2,L3,L4	1uH	L0805	DNP	Panasonic	ERJ-3GEY0R00V
53	8	R16,R18,R20,R22,R30,R32,R34,R36	0	RES0402	DNP	Panasonic	ERJ-2GE0R00X
56	4	R39,R40,R43,R44	82	RES0603	DNP	BOURNS	CR0603-FX-82R0ELF
57	4	R41,R42,R45,R46	49.9	RES0603	DNP	Yageo America	9C06031A49R9FKHFT
58	2	R47,R48	100	RES0603	DNP	Panasonic	ERJ-3EKF1000V
59	4	R49,R50,R51,R52	130	RES0603	DNP	Panasonic	ERJ-3EKF1300V
60	8	R53,R54,R55,R56,R57,R58,R59,R60	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
63	4	R75,R77,R78,R144	10K	RES0603	DNP	Panasonic	ERJ-3GEYJ103V
70	6	R146,R149,R151,R152,R164,R168	ZERO	RES0603	DNP		
72	1	R165,R147,R150	10.0K	RES0603	DNP	Panasonic	ERJ-3EKF1002V
37	1	PIM1	PIM CONN	TH_CONN_PIM100	DNP		
81	2	TP3,TP4	TEST POINT	TH_TP_60D40	DNP	FCI	68000-201HLF

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