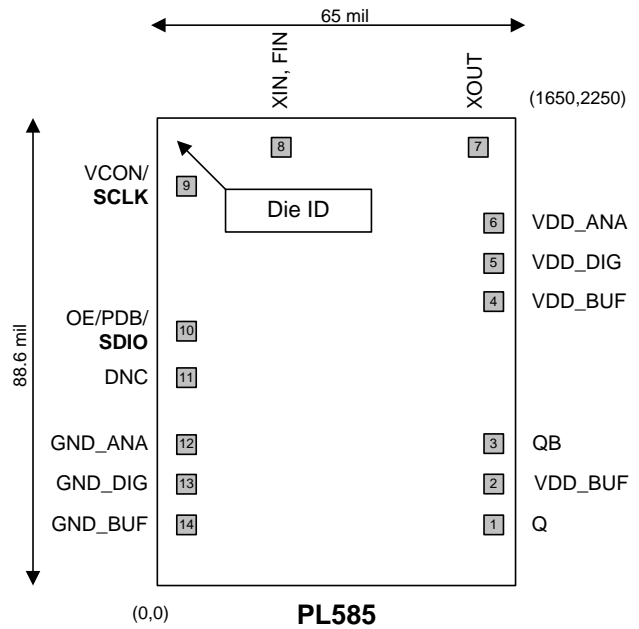


## 19MHz to 250MHz Low Phase-Noise VCXO

### FEATURES

- < 0.6ps RMS phase jitter (12kHz to 20MHz) at 155.52MHz
- 30ps max peak to peak period jitter
- Ultra Low-Power Consumption
  - < 90mA @155MHz PECL output
  - < 10µA at Power Down (PDB) Mode
- Input Frequency:
  - Fundamental Crystal: 19MHz to 40MHz
- Output Frequency:
  - 19MHz to 250MHz output.
- Output type: LVPECL
- High Linearity VCXO: <10% linearity
- Pullability: ±150 ppm
- Programmable OE input polarity selection.
- Power Supply: 3.3V, ±10%
- Operating Temperature Ranges:
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
- Available in Die or Wafer

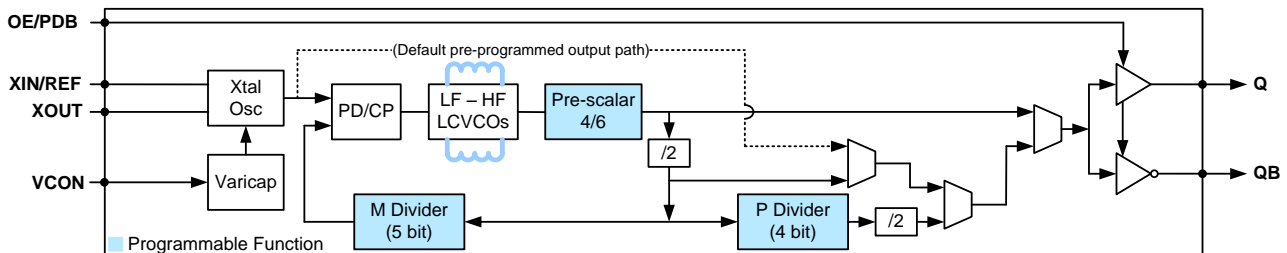
### PIN CONFIGURATION

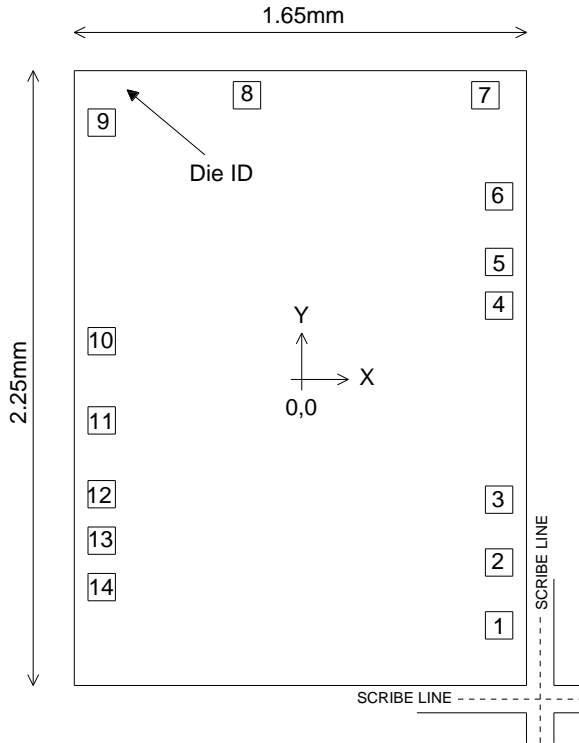


### DESCRIPTION

The PL585-28 is a Dual LC core monolithic IC clock, capable of maintaining sub-picoseconds RMS phase jitter, while covering a wide frequency output range up to 250MHz, without the use of external components. The high performance and high frequency output is achieved using a low cost fundamental crystal of between 19MHz and 40 MHz. The PL585-28 is designed to address the demanding requirements of high performance applications such as Fiber Channel, serial ATA, Ethernet, SAN, SONET/SDH, etc.

### BLOCK DIAGRAM



**19MHz to 250MHz Low Phase-Noise VCXO**
**DIE SPECIFICATIONS**


Chip size, active area	1.650mm x 2.250mm
Chip thickness	200 $\mu$ m $\pm$ 20 $\mu$ m
PAD size	80 $\mu$ m x 80 $\mu$ m
Scribe Line Dimension	X = 80 $\mu$ m Y = 80 $\mu$ m
Chip Base	GND level
<u>Die ID:</u> PL585-28DC	C685B C9-99-99-9

**PAD ASSIGNMENT AND DESCRIPTION (The X/Y coordinates indicate pad centers)**

Name	Pad #	X ( $\mu$ m)	Y ( $\mu$ m)	Description
Q	1	+726	-905	Output buffer
VDD_BUF	2	+726	-677	VDD connection for buffer circuitry
QB	3	+726	-449	Output buffer
VDD_BUF	4	+726	+265	VDD connection for buffer circuitry
VDD_DIG	5	+726	+427	VDD connection for digital circuitry
VDD_ANA	6	+726	+665	VDD connection for analog circuitry
XOUT	7	+678	+1031	Output connection to crystal
XIN	8	-195	+1031	Crystal input connection
VCON/SCLK	9	-726	+935	Analog voltage pin for the VCXO. The serial interface uses this pin for the serial clock input (SCLK), during programming.
OE/PDB/SDIO	10	-726	+131	This pin may be programmed as output enable (OE), or power-down (PDB) pin. The serial interface uses this pin for the serial data input (SDIO) during programming. This pin incorporates an Internal pull-up resistor of 60K $\Omega$ for OE, PDB operations.
DNC	11	-726	-155	Do not connect
GND_ANA	12	-726	-425	GND connection for analog circuitry
GND_DIG	13	-726	-593	GND connection for digital circuitry
GND_BUF	14	-726	-761	GND connection for buffer circuitry

## 19MHz to 250MHz Low Phase-Noise VCXO

### FUNCTIONAL DESCRIPTION

PL585 family of products is an advanced, programmable LCVCO clock IC that is designed to meet the most stringent performance specifications for phase noise, jitter, and power consumption.

There are two main types of VCOs, a) Ring Oscillator, b) LC Tank oscillator. An LCVCO is made up of an LC tank oscillator. Although a Ring Oscillator has very good performance, and has a good tuning range, its phase noise and jitter performance, in particular at higher frequencies, degrades.

On the other hand, an LCVCO has an outstanding phase noise and jitter performance, even at higher frequencies. PL585 family of products takes advantage of this state of the art technology, and incorporates the LC tank on-chip, for optimal performance.

PL585 family of products exhibit very low phase noise/phase jitter and peak to peak jitter, wide tuning range, and very low-power. All members of the PL585 family accept a low-cost fundamental crystal input of 19MHz to 40MHz, and its flexible core is capable of producing any output frequency between 19MHz to 800MHz. The PL585-28 specifically is limited to 250MHz. See the PL585-88 for operation up to 800MHz.

### PLL Programming

The PLL in the PL585 family is fully programmable. The PLL is equipped with a Pre-Scalar to divide down the VCO frequency, and a 5-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 4-bit post VCO divider (P-Counter), to achieve the desired output frequency.

### OE (Output Enable)

The OE pin in PL585 family, through programming, can be configured to support OE pin activation with a logic '1' or logic '0', to provide you with the desired enable polarity.

OE Select (Programmable)	OE	State
0	0 (Default)	Output enabled
	1	Tri-state
1 (Default)	0	Tri-state
	1 (Default)	Output enabled

The OE pin incorporates a 60K $\Omega$  resistor to either pull-up or pull-down to the default state, when the OE pad is left open.

**19 MHz to 250MHz Low Phase-Noise VCXO**
**ELECTRICAL SPECIFICATIONS**
**1. ABSOLUTE MAXIMUM RATINGS**

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature (industrial temperature)*	$T_{AI}$	-40	85	°C
Ambient Operating Temperature (commercial temperature)	$T_{AC}$	0	70	°C
Junction Temperature	$T_J$		125	°C
ESD Protection, Machine Model		200		V
ESD Protection, Human Body Model		2		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

**2. GENERAL ELECTRICAL SPECIFICATIONS**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	$I_{DDQ}$	LVPECL, 155.52MHz, 3.3V			90	mA
Supply Current, Dynamic PDB Enabled		PDB = 0, 3.3V			10	uA
Output Enable Time	$t_{OE}$	OE logic 0 to logic 1, $T_a=25^\circ\text{C}$ . Add one clock period to this measurement for a usable clock output.			50	ns
Power Up Time	$T_{PU}$	PDB logic 0 to logic 1, $T_a=25^\circ\text{C}$ .			10	ms
Operating Voltage	$V_{DD}$		2.97	3.3	3.63	V
Power Up Ramp Rate	$t_{PU}$	Time for $V_{DD}$ to reach 90% $V_{DD}$ . Power ramp must be monotonic.	0.1		100	ms
Auto-Calibration Time	$t_{AC}$	At power up			10	ms
Output Clock Duty Cycle		@ $V_{DD} - 1.3V$	45	50	55	%

**19 MHz to 250MHz Low Phase-Noise VCXO**
**3. VOLTAGE CONTROLLED CRYSTAL OSCILLATOR**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCXO Pullability		VCON=1.65V, $\pm 1.65V$ XTAL $C_1 > 10fF$ and $C_0/C_1 < 250$	$\pm 150$			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull Range Linearity					10	%
VCON Pin Input Impedance			10			M $\Omega$
VCON Modulation BW		$0V \leq VCON \leq 3.3V$ , -3dB	18			kHz

**4. CRYSTAL SPECIFICATIONS**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	19		40	MHz
Crystal Load	$C_{L\_Crystal}$	$V_{DD} = 3.3V$ , VCON = 1.65V		8.5		
Shunt Capacitance	$C_{0\_Crystal}$				3.5	pF
Crystal Pullability	$C_0/C_1$	AT cut	250			--
Recommended ESR	$R_E$	AT cut			50	$\Omega$

**5. JITTER SPECIFICATIONS**

PARAMETERS	FREQUENCY	CONDITIONS	MIN	TYP	MAX	UNITS
RMS Phase Jitter	155.52MHz	10kHz to 20MHz, XIN=38.88MHz		0.56		ps
Period Jitter, Pk-to-Pk	155.52MHz	10K cycles, XIN=38.88MHz		25		ps

**6. PHASE NOISE SPECIFICATIONS**

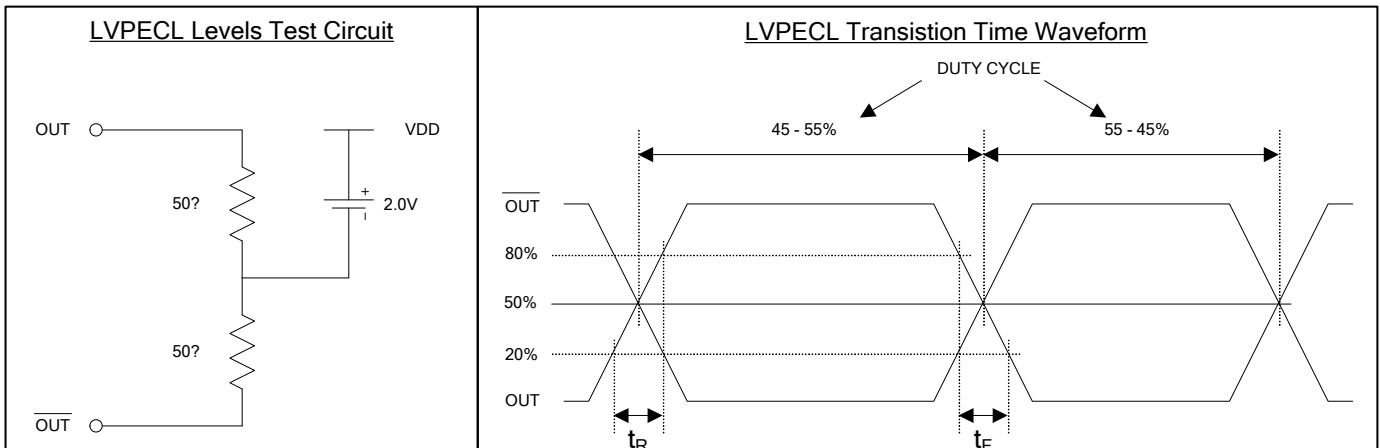
PARAMETERS	Freq. (MHz)	@ 10Hz	@ 100Hz	@ 1KHz	@ 10KHz	@ 100KHz	@ 1MHz	@ 10MHz	UNITS
Phase Noise, relative to carrier (typical)	155.52	-56	-86	-112	-123	-127	136	147	dBc/Hz

Note: Phase Noise measured at VCON = 1.65V

**19MHz to 250MHz Low Phase-Noise VCXO**

**7. LVPECL OUTPUTS (Q, QB)**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH}$	Q, QB	2.275	2.350	2.420	V
Output Low Voltage	$V_{OL}$	Standard LVPECL Termination, $V_{DD} = 3.3V$	1.490	1.600	1.680	V
Output Frequency	$F_{out}$	3.3V	19		250	MHz
Output Rise, Fall Times	$t_r, t_f$	20% - 80% of $Q_{pp}/QB_{pp}$		200	300	ps
Output Voltage Swing	$V_{pp}$	Q, QB	550	800	900	mV



**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

2180 Fortune Drive, San Jose, CA 95131, USA  
Tel: (408) 944-0800 Fax: (408) 474-1000

**PART NUMBER**

The order number for this device is a combination of the following:  
Part number, Package type, Thickness and Operating temperature range

**PL585-28 XX**

Part Number \_\_\_\_\_

**Packaging Option** \_\_\_\_\_

D = Die  
W = Wafer

**Temperature Range** \_\_\_\_\_

C=Commercial (0°C to 70°C)

Order Number P/N	Output Frequency Range	Packaging Option
<b>PECL</b>		
PL585-28DC	≤250MHz	Waffle Pack (Die)
PL585-28WC	≤250MHz	Wafer

Micrel Inc., reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Micrel is believed to be accurate and reliable. However, Micrel makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

**LIFE SUPPORT POLICY:** Micrel's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Micrel Inc.