(Preliminary) Analog Frequency Multiplier

PL565-37/38 VCXO Family

PRODUCT DESCRIPTION

The Analog Frequency Multiplier (AFM) is the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase-locked loop (PLL), in CMOS technology.

The PL565-37/38 products can achieve up to 250 MHz output frequency with little jitter or phase noise deterioration. In addition, the low frequency input crystal requirement makes the AFMs the most affordable high-performance timing-source in the market.

Product Selector

Part Number	Output Type
PL565-38	PECL Output
PL565-37	CMOS Output

FEATURES

- Non-PLL frequency multiplication
- Input frequency from 30-62.5 MHz
- Output frequency from 120-250 MHz
- Low phase noise and jitter (equivalent to fundamental crystal at the output frequency)
- Ultra-low jitter
  - RMS phase jitter < 0.25 ps (12kHz-20MHz)
  - RMS period jitter < 25 ps
- Low phase noise
  - -147 dBc/Hz @100kHz offset from 155.52 MHz
  - -157 dBc/Hz @10MHz offset from 155.52 MHz
- High linearity pull range (typ. 5%)
- +/- 120 PPM pullability VCXO
- Low input frequency eliminates the need for expensive crystals
- Differential output levels PECL or single-ended CMOS
- Single 3.3V, ±10% power supply
- Optional industrial temperature range (-40°C to +85°C)

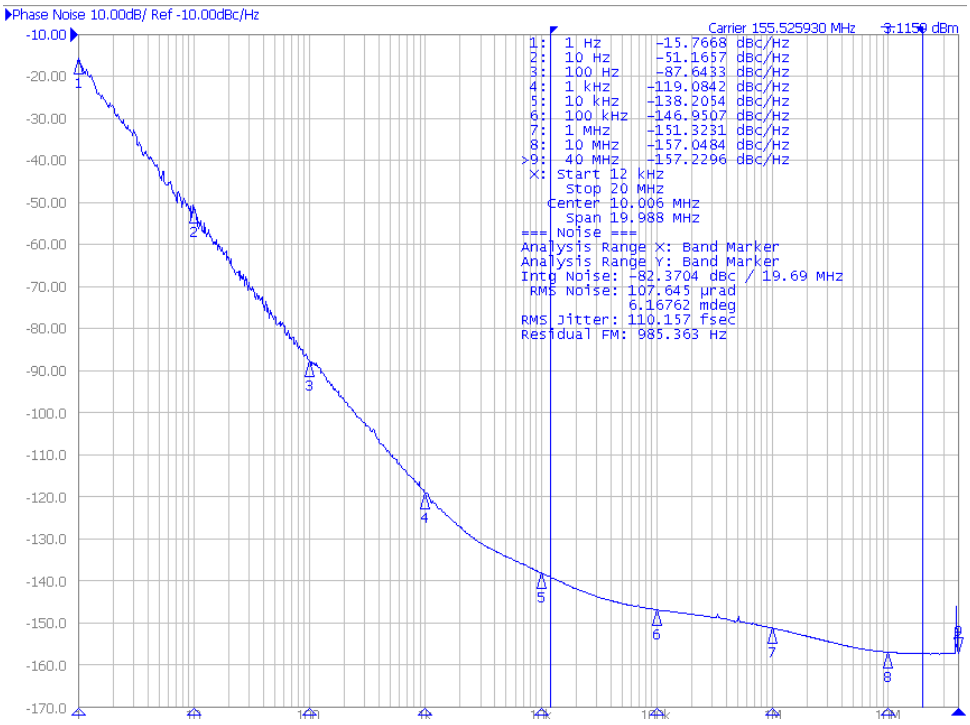


Figure 1: 4X AFM Phase Noise at 155.52MHz

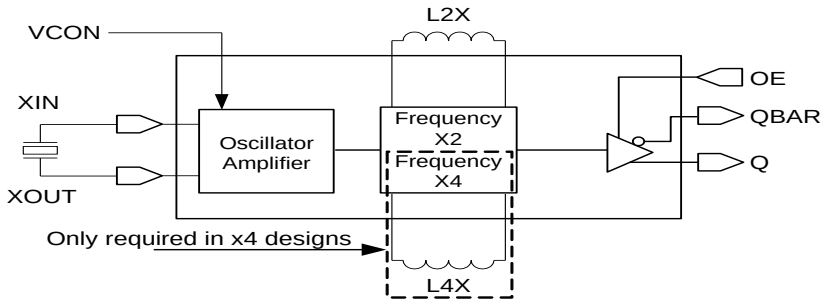


Figure 2: Block Diagram of VCXO AFM

Figure 3 shows the period jitter histogram of the 4X Analog Frequency Multiplier at 311.04 MHz, while Figure 4 shows the very low rejection levels of sub-harmonics that correspond to the exceptionally low jitter performance.

Figure 3: Period Jitter Histogram at 155.52 MHz
Analog Frequency Multiplier (4x)
with 38.88MHz crystal

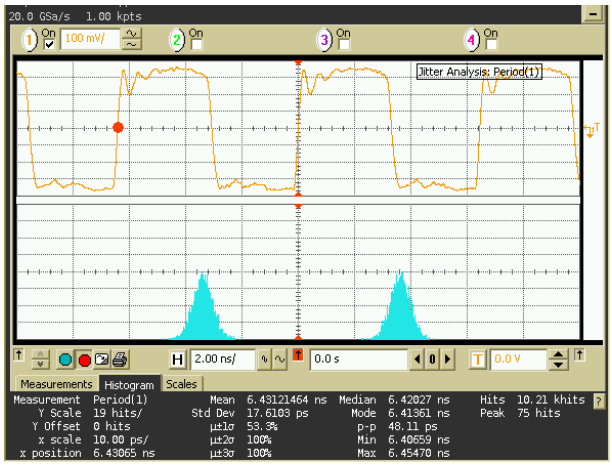
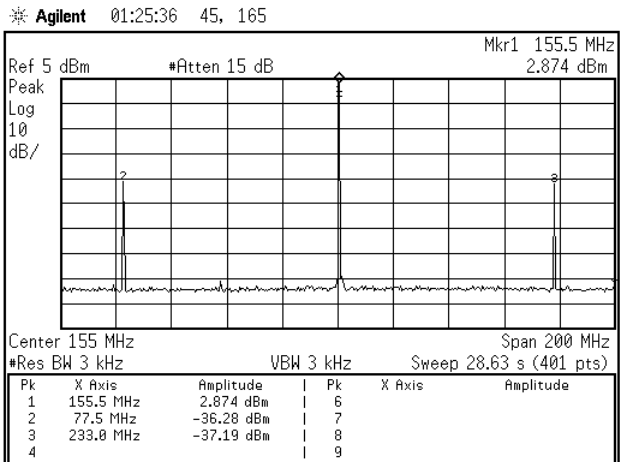


Figure 4: Spectrum Analysis at 155.52 MHz
Analog Frequency Multiplier (4x)
with sub-harmonics below –39 dBc



OE LOGIC SELECTION

OUTPUT	OESEL	OE	Output State
LVPECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
		1 (Default)	Enabled
LVCMOS	0 (Default)	0	Tri-state
		1 (Default)	Enabled
	1	0 (Default)	Enabled
		1	Tri-state

OESEL and OE: Connect to VDD or leave floating to set to "1", connect to GND to set to "0".
Internally set to default through pull-down / -up.

PRODUCT SELECTION GUIDE

FREQUENCY VERSUS PHASE NOISE PERFORMANCE

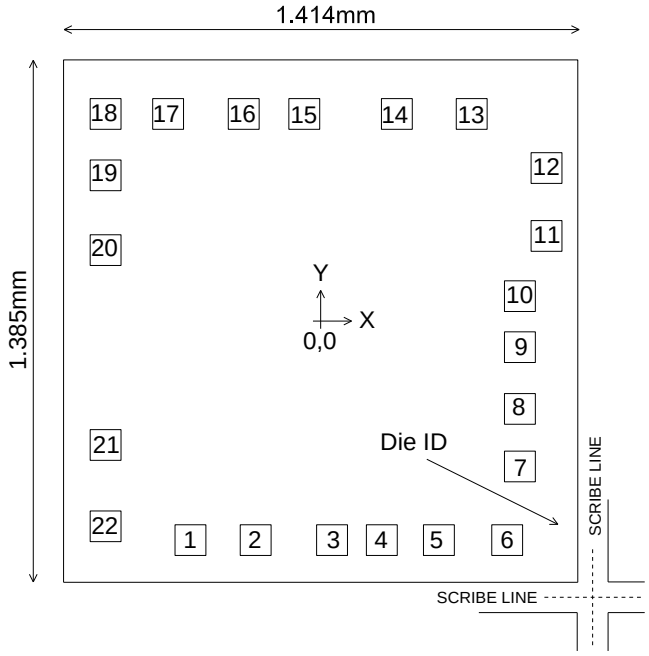
Part Number	Input Frequency Range (MHz)	Analog Frequency Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise at Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz
PL565-37	30 - 60	4	120 - 250	LVCMOS	155.52	-51	-88	-119	-138	-147	-151	-157
PL565-38	30 - 60	4	120 - 250	LVPECL	155.52	-51	-88	-119	-138	-147	-151	-157

JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Output Freq. (MHz)	RMS Period Jitter (ps)			Peak to Peak Period Jitter (ps)			RMS Accumulated (L.T.) Jitter (ps)			RMS Phase Jitter 12kHz to 20MHz (ps)			Spectral Specifications / Sub-harmonic Content (dBc), Frequency (MHz)						
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Carrier Freq. (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
PL565-37	155		18	25		50	100			25		0.25		155.52	-75	-39			-40	-75
PL565-38	155		18	25		50	100			25		0.25		155.52	-75	-39			-40	-75

Note: Agilent 5052B was used for phase jitter measurements.
Spectral specifications were obtained using Agilent E7401A.

DIE SPECIFICATIONS



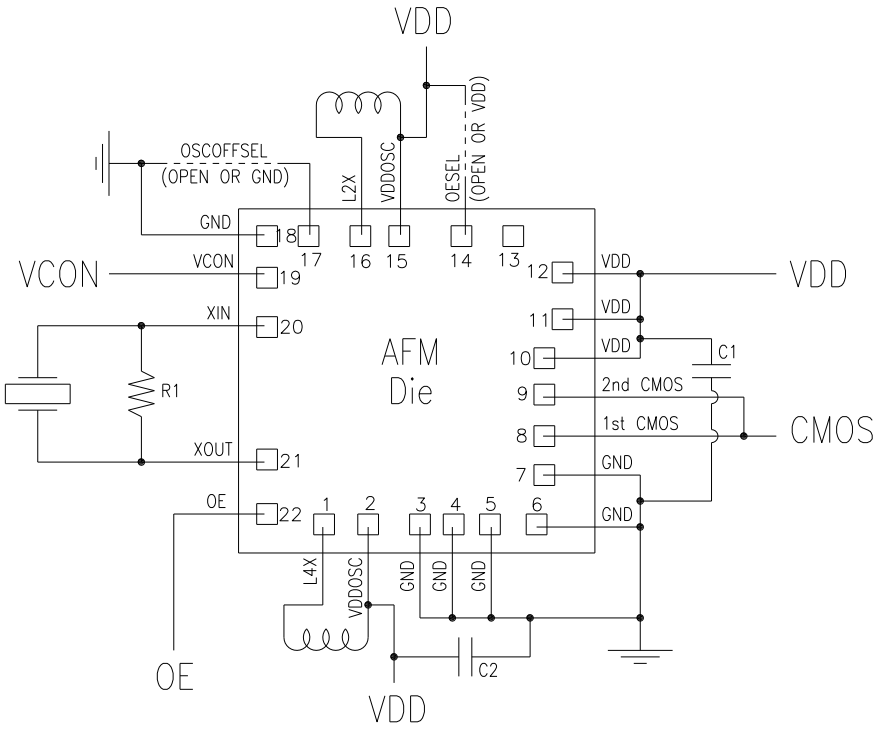
Chip size, active area	1.414mm x 1.385mm
Chip thickness	200 ± 20µm
PAD size	80µm x 80µm
Scribe Line Dimension	X = 80µm Y = 80µm
Chip Base	GND level
Die ID: PL565-37DC PL565-38DC	 C561A CCCCCCC C561A DDDDDDD

PAD ASSIGNMENT AND DESCRIPTION (The X/Y coordinates indicate pad centers)

Name	Pad Assignment*			Type	Description
	Pad #	X (µm)	Y (µm)		
L4X	1	-352	-557	I	External inductor connection
VDDOSC	2	-183	-557	P	VDD connection
GNDANA	3	+15	-557	P	GND connection
GNDANA	4	+144	-557	P	GND connection
GNDBUF	5	+292	-557	P	GND connection
GNDBUF	6	+469	-557	P	GND connection
GNDBUF	7	+502	-365	P	GND connection
OUTB	8	+502	-215	O	-37: LVCMOS 2nd in-phase output -38: LVPECL complementary output
OUT	9	+502	-54	O	-37: LVCMOS output, -38: LVPECL output
VDDBUF	10	+502	+79	P	VDD connection
VDDBUF	11	+571	+236	P	VDD connection
VDDANA	12	+571	+413	P	VDD connection
N.C.	13	+377	+554		
OESEL	14	+183	+554	I	OE style selection pin
VDDOSC	15	-57	+554	P	VDD connection
L2X	16	-214	+554	I	External inductor connection
OSCOFFSEL	17	-410	+554	I	Oscillator Off selection pin
GNDOSC	18	-572	+554	P	GND connection
VCON	19	-572	+394	I	Control voltage input
XIN	20	-572	+199	I	Crystal Input pad
XOUT	21	-572	-309	O	Crystal Output pad
OE	22	-572	-521	I	Output Enable input

*** Note: Pad coordinates referenced to the center of the die.**

AFM DIE APPLICATION CIRCUIT FOR PL565-37 (LVCMOS)



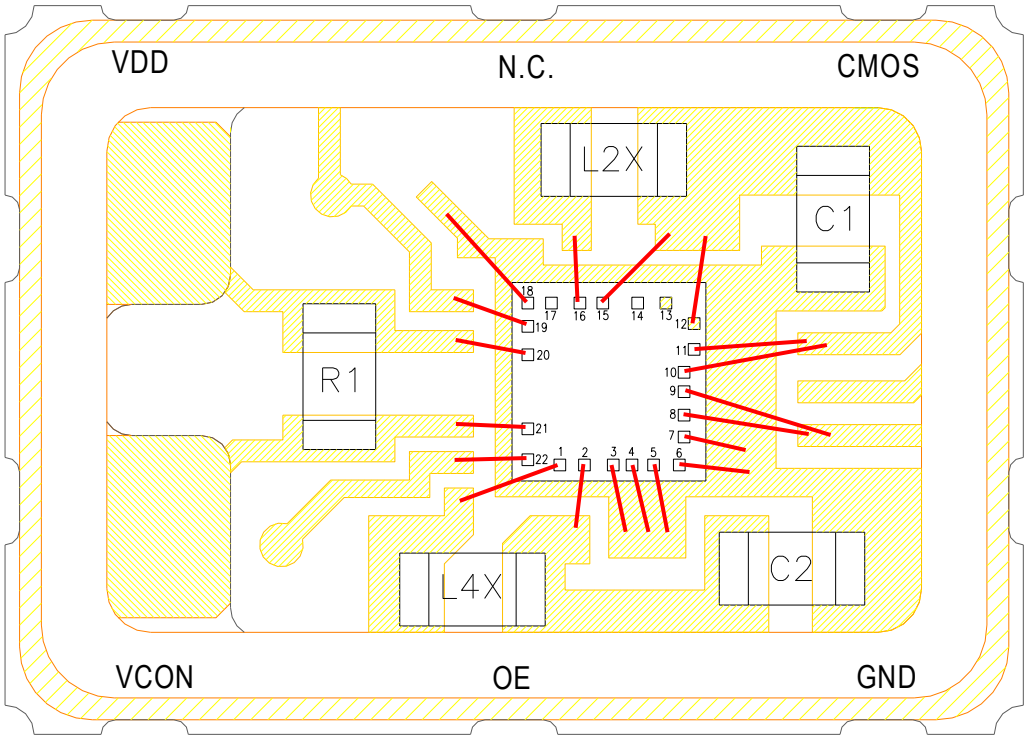
C1, C2: Power Supply Decoupling. The advised value is 0.01µF.

R1: Oscillator Amplitude Control. The advised value is 10KΩ.

L2X, L4X: Multiplier Tuning. Contact factory for optimum values.

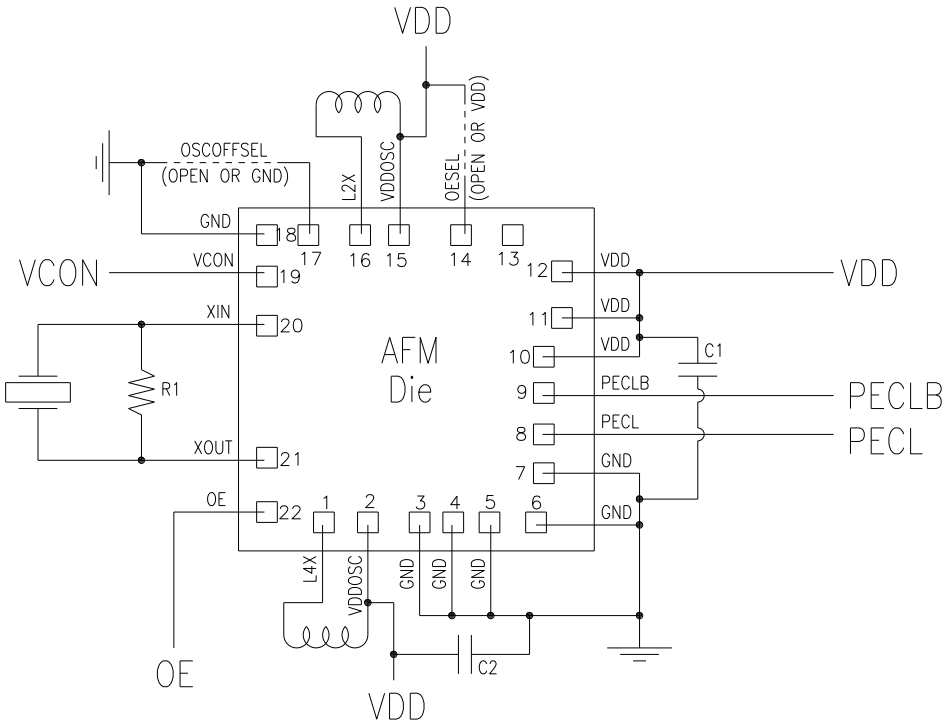
1st and 2nd CMOS outputs are 8mA drive each. They are in-phase and connected together they make a 16mA drive output.
16mA drive is advised for driving 50Ω PCB traces.

A 7x5mm ceramic substrate was designed to assemble and operate the AFM die at optimum performance:



Substrate part number: Kyocera KD-VA9501

AFM DIE APPLICATION CIRCUIT FOR PL565-38 (LVPECL)

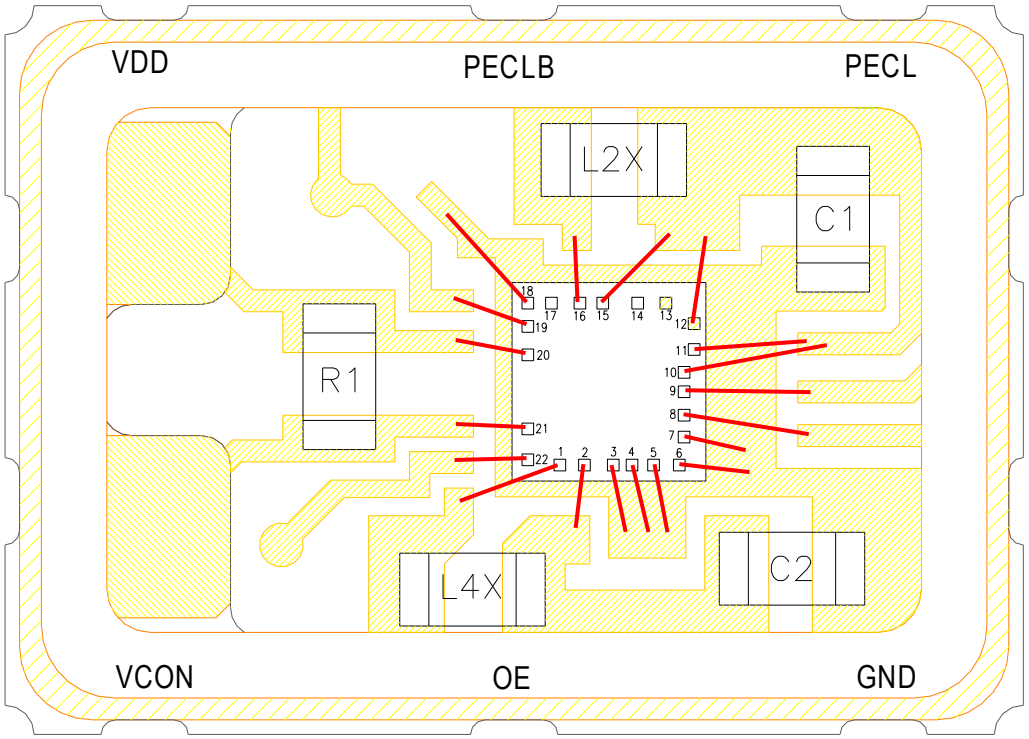


C1, C2: Power Supply Decoupling. The advised value is 0.01µF.

R1: Oscillator Amplitude Control. The advised value is 10KΩ.

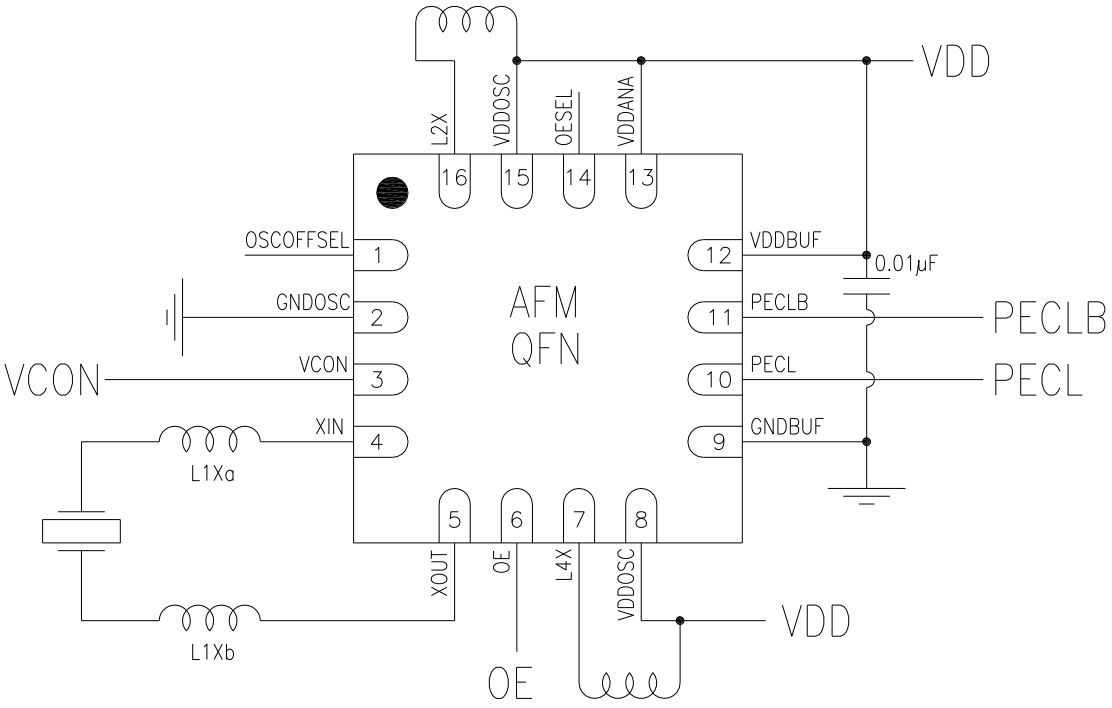
L2X, L4X: Multiplier Tuning. Contact factory for optimum values.

A 7x5mm ceramic substrate was designed to assemble and operate the AFM die at optimum performance:

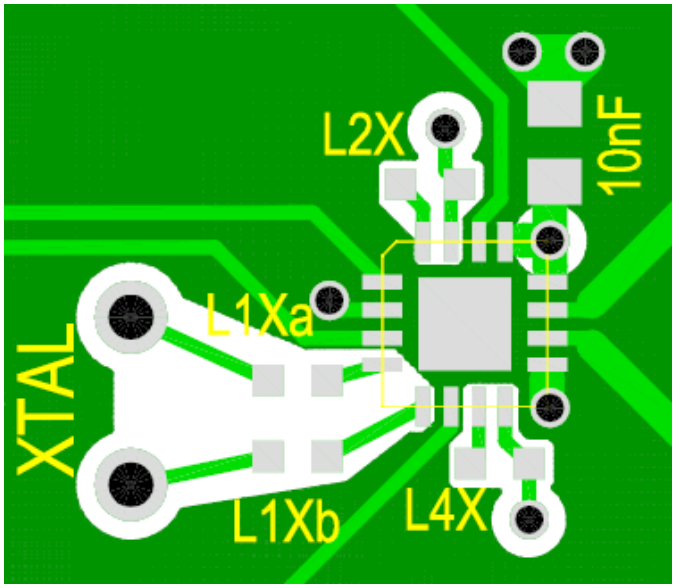


Substrate part number: Kyocera KD-VA9501

AFM QFN PACKAGE APPLICATION CIRCUIT



RECOMMENDED PCB LAYOUT



- Avoid ground planes underneath the crystal and inductor traces to limit parasitic capacitance.
- Add bypass capacitor close to VDDBUF pin.
- Avoid bypass capacitors near VDDOSC pins to lower cross-talk of unwanted frequencies.
- L1X(a,b) can be used to increase the VCXO pulling range. Using a ferrite core inductor limits the oscillation amplitude which can have a positive effect on phase noise.
- L2X and L4X tune the frequency multiplier tank circuits. They need to be wire wound inductors with high Q-factor, preferably >20.
- The large center pad is the “thermal relief” pad and can be connected to ground.

INDUCTOR VALUE OPTIMIZATION

The required inductor values for the best performance depend on the operating frequency, and the board layout or module specifications. The listed values in this datasheet are based on the calculated parasitic values from Micrel's evaluation board design. These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X / L4X and adjacent VDDOSC pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

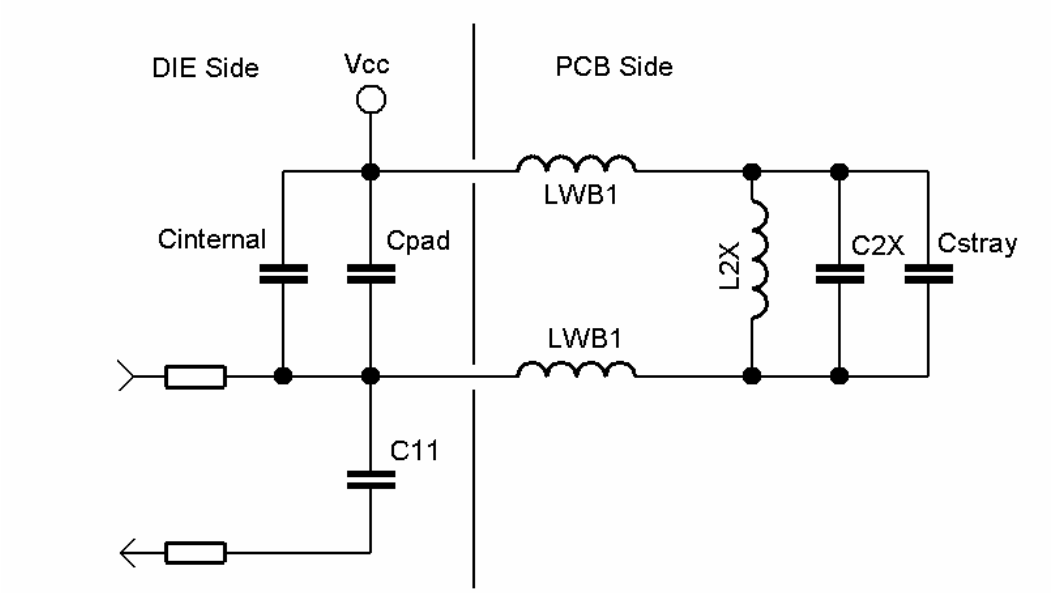


Figure 10: Diagram Representation of the Related System Inductance and Capacitance

DIE SIDE
- Cinternal at L2X = 34.125 pF,
  at L4X = 16.50 pF
- Cpad = 1.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, the following amplifier stage

PCB side
- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 0.5 pF, Stray capacitance
- L2X (L4X) = 2x or 4x inductor
- C2X (C4X) = range (0.1 to 2.7 pF), Fine tune the tank, if used.

Work out the resonance of this network and you have a good first guess for the required inductor values for optimum performance. Non-linear behavior at large signal amplitudes can shift the tank resonance significantly, especially at the L2X side, to a lower frequency than the calculation suggests.

CRYSTAL SPECIFICATIONS & TUNING PERFORMANCE

CRYSTAL SPECIFICATIONS						TUNING PERFORMANCE					
PART NUMBER	CRYSTAL RESONATOR FREQUENCY (FXIN)	MODE	CL (xtal)		ESR (R_E)	CRYSTAL			TUNING (Typical)		
			CONDI-TIONS	TYP	MAX	CRYSTAL FREQ (MHz)	C0	C1	C0/C1	VC: 1.65V → 0V	VC: 1.65V → 3.3V
PL565-37/38	30 to 62.5MHz	Funda-mental	At VCON = 1.65V	5pF	30Ω	30.72	2.8pF	12.4fF	228	-167ppm	+176 ppm
						30.72	4.5pF	19.1fF	236	-163 ppm	+167 ppm
						38.88	5.1pF	20.9fF	242	-131 ppm	+98 ppm
						38.88	5.3pF	25.6fF	207	-157 ppm	+141 ppm
						77.76	2.0pF	6.7fF	305	-92 ppm	+110 ppm

Note: Non specified parameters can be chosen as standard values from crystal suppliers.
CL ratings larger than 5pF require a crystal frequency adjustment. Request detailed crystal specifications from Micrel.

VOLTAGE CONTROL SPECIFICATION

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		XTAL C_0 /C_1 <300	200			ppm
CLK Output Pullability		VCON= 1.65V, ± 1.65V XTAL C_0 /C_1 <300	±100	±120		ppm
Linearity				5	10	%
VCON Input Impedance			10			MΩ
VCON Modulation BW		0V < VCON < 3.3V, -3dB	16			kHz

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

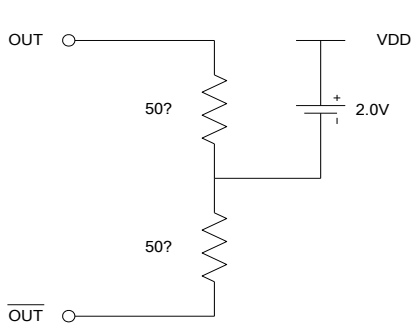
PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, DC	V_I	GND-0.5	V_{DD}+0.5	V
Output Voltage, DC	V_O	GND-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature, Industrial	T_{A_I}	-40	+85	°C
Ambient Operating Temperature, Commercial	T_{A_C}	0	+70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the dev ice at these or any other conditions above the operational limits noted in this specification is not implied.

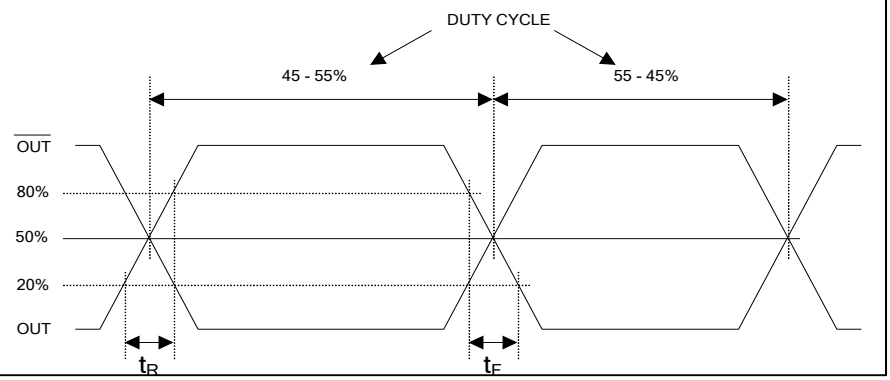
LVPECL ELECTRICAL CHARACTERISTICS FOR PL565-38

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	I_{DD}	Fout = 155.52MHz		75	80	mA
Operating Voltage*	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ V_{DD} – 1.3V	45	50	55	%
Short Circuit Current				±50		mA
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V)	V_{DD}-1.025			V
Output Low Voltage	V_{OL}				V_{DD}-1.620	V
Clock Rise Time	t_r	@ 20/80%		0.25	0.45	ns
Clock Fall Time	t_f	@ 80/20%		0.25	0.45	ns

LVPECL Levels Test Circuit



LVPECL Transistion Time Waveform



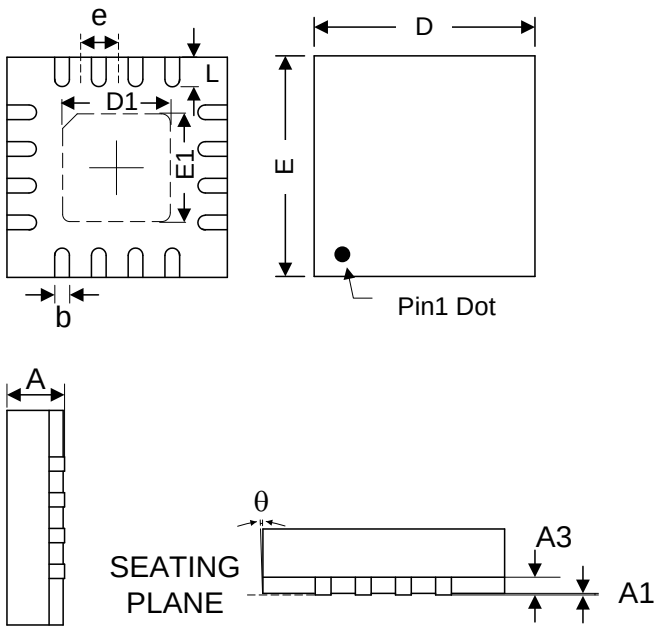
LVCMOS ELECTRICAL CHARACTERISTICS FOR PL565-37

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	I_{DD}	At 150MHz, 15pF load		20	30	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output High Voltage (LVTTL)	$V_{OH3.3}$	I_{OH} = -8mA, 3.3V	2.4			V
Output Low Voltage (LVTTL)	$V_{OL3.3}$	I_{OL} = 8mA, 3.3V			0.4	V
Output High Voltage (LVCMOS)	$V_{OHC3.3}$	I_{OH} = -4mA, 3.3V	V_{DD} – 0.4			V
Output Drive Current	$I_{OSD3.3}$	V_{OL} = 0.4V, V_{OH} = 2.4V (per output), 3.3V	8			mA
Output Clock Rise/Fall Time	T_r,T_f	10% / 90% V_{DD}, 10 pF load, 1 output		1.2	1.6	ns
		10% / 90% V_{DD}, 15 pF load, 2 outputs		1.0	1.5	ns
Output Clock Duty Cycle		Measured @ 50% V_{DD}	45	50	55	%

PACKAGE INFORMATION

QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e		0.50BSC	



For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL565-3X X X X

PART NUMBER

NONE= TUBE
R= TAPE AND REEL

PACKAGE TYPE
Q= QFN-16L
D= Die

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Order Number	Marking	Package Option
PL565-37DC PL565-38DC	-	Die Only
PL565-37QC	P565 37(I) LLL	QFN – Tube
PL565-37QC-R		QFN – Tape and Reel
PL565-38QC	P565 38(I) LLL	QFN – Tube
PL565-38QC-R		QFN – Tape and Reel

Marking Notes: "LLL", "LLLLL" represents the production lot number

ORDERING INFORMATION