PIC18-Q83/84 Family Programming Specification

Introduction

This programming specification describes an SPI-based programming method for the PIC18-Q83/84 family of microcontrollers. The Programming Algorithms section describes the programming commands, programming algorithms and electrical specifications used in that particular programming method. Appendix B contains individual part numbers, device identification and checksum values, pinout and packaging information, and Configuration Bytes.

Important:

- This is an SPI-compliant programming method with 8-bit commands.
- The low-voltage entry code is now 32 clocks and MSb first, unlike earlier PIC18 devices, which had 33 clocks and LSb first.

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1. Overview

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage ICSP interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM, dedicated User ID locations and the Configuration Bytes.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in the table below. For pin locations and packaging information, refer to the table in the **"Appendix B"** section.

Table 1-1. Pin Descriptions During Programming

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ISCPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ISCPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}/V_{PP}$	Program/Verify mode	I(1)	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note:

1. The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

1.3 Hardware Requirements

1.3.1 High-Voltage ICSP™ Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: One for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

1.3.2 Low-Voltage ICSP™ Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the device operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to the programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP™ Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and can be used to program the device.

Important:

- The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
- While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled regardless of the MCLRE bit. Also, the $\overline{MCLR}$ pin can no longer be used as a general purpose input.

1.4 Write and/or Erase Section

Erasing or writing is selected according to the command used to begin operation (see Table 3-1). The terminologies used in this document, related to erasing/writing to the program memory, are defined in the table below.

Table 1-2. Programming Terms

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.4.1 Erasing Memory

Memory is erased by 128-word pages or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the data memory erase is determined by the size of the data memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Page Erase and Write requirements.

Page erasing pertains to PFM and User ID memory only. The configuration and data memory will be erased by the Bulk Erase command. For self-write operations, each byte write to data memory includes an automatic erase cycle for the location about to be programmed.

1.4.2 Writing Memory

Memory is written one word at a time. The duration of the write is determined internally.

Note: The size of the word is of 16 bits for the Program Flash Memory and of eight bits for the EEPROM, but the same 24-bit payload is used for both memory regions.

2. Memory Map

This section provides details on how the program memory and EEPROM are organized for this device.

Figure 2-1. Program and Data EEPROM Memory Map

Rev. 40-000101F
4/20/2017

Address	Device	
	PIC18Fx6Q83/84	PIC18Fx7Q83/84
00 0000h to 00 3FFFh	Program Flash Memory (32 KW)(1)	Program Flash Memory (64 KW)(1)
00 4000h to 00 7FFFh		
00 8000h to 00 FFFFh		
01 0000h to 01 FFFFh	Not Present(2)	
02 0000h to 1F FFFFh		Not Present(2)
20 0000h to 20 001Fh	User IDs (32 Words)(3)	
20 0020h to 2B FFFFh	Reserved	
2C 0000h to 2C 00FFh	Device Information Area (DIA)(3,5)	
2C 0100h to 2F FFFFh	Reserved	
30 0000h to 30 0022h	Configuration Bytes(3)	
30 0023h to 37 FFFFh	Reserved	
38 0000h to 38 03FFh	Data EEPROM (1024 Bytes)	
38 0400h to 3B FFFFh	Reserved	
3C 0000h to 3C 000Ah	Device Configuration Information(3,4,5)	
3C 000Bh to 3F FFBh	Reserved	
3F FFFCh to 3F FFDh	Revision ID (1 Word)(3,4,5)	
3F FFEh to 3F FFFh	Device ID (1 Word)(3,4,5)	

Notes: 1. Storage Area Flash is implemented as the last 128 Words of User Flash, if enabled.

2. The addresses do not roll over. The region is read as '0'.

3. Not code-protected.

4. Hard-coded in silicon.

5. This region cannot be written by the user and it is not affected by a Bulk Erase.

2.1 User ID Location

The user may store identification information (User ID) in 32 designated locations. The User ID locations are mapped to addresses 20 0000h-20 001Fh. Each location is 16 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 16-bit Device ID Word is located at the address 3F FFFEh and the 16-bit Revision ID is located at the address 3F FFFCh. These locations are read-only and cannot be erased or modified. See the Device ID and Revision ID registers for more details.

2.3 Device Configuration Information (DCI)

The Device Configuration Information (DCI) is a dedicated region in the memory that holds information about the device, which is useful for programming and bootloader applications. The data stored in this region are read-only and cannot be modified/erased. Refer to the table below for complete DCI table addresses and description.

Table 2-1. Device Configuration Information

Address	Name	Description	Value		Units
			PIC18F26/46/56Q83/84	PIC18F27/47/57Q83/84	
3C0000h	ERSIZ	Erase page size	128		Words
3C0002h	WLSIZ	Number of write latches per row	0		Words
3C0004h	URSIZ	Number of user-erasable pages	256	512	Pages
3C0006h	EESIZ	Data EEPROM memory size	1024		Bytes
3C0008h	PCNT	Pin count	28/40(1)/48	28/40(1)/48	Pins

Note:

1. Pin Count value of 40 is used for 44-pin parts as well.

2.4 Configuration Bytes

The devices have 35 Configuration Bytes, starting at address 30 0000h. The Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, consider the following Configuration bits:

1. **LVP: Low-Voltage Programming Enable bit**
   - 1 = ON: Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. The MCLRE Configuration bit is ignored.
   - 0 = OFF: High voltage on $\overline{MCLR}/V_{PP}$ must be used for programming.

Important: The LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state. For more information, refer to 3.1.2 Low-Voltage Programming (LVP) Mode.

2. **MCLRE: Master Clear ($\overline{MCLR}$) Enable bit**
   - If LVP = 1: RE3 pin function is $\overline{MCLR}$

  - If LVP = 0
    - 1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
    - 0 = $\overline{\text{MCLR}}$ pin function is a port-defined function
3. **$\overline{\text{CP}}$: User NVM Program Memory Code Protection bit**
  - 1 = OFF: User NVM code protection is disabled
  - 0 = ON: User NVM code protection is enabled

For more information on code protection, see 3.3 Code Protection.

2.5 Device ID

Name: DEVICEID
Offset: 3FFFFEh

Device ID Register

Bit	15	14	13	12	11	10	9	8
	DEV[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bits 15:0 – DEV[15:0] Device ID

Device	Device ID
PIC18F26Q83	A306h
PIC18F26Q84	A300h
PIC18F27Q83	9909h
PIC18F27Q84	9903h
PIC18F46Q83	A307h
PIC18F46Q84	A301h
PIC18F47Q83	990Ah
PIC18F47Q84	9904h
PIC18F56Q83	A308h
PIC18F56Q84	A302h
PIC18F57Q83	990Bh
PIC18F57Q84	9905h

2.6 Revision ID

Name: REVISIONID
Offset: 3FFFFCh

Revision ID Register

Bit	15	14	13	12	11	10	9	8
	1010[3:0]				MJRREV[5:2]			
Access	R	R	R	R	R	R	R	R
Reset	1	0	1	0	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bits 15:12 – 1010[3:0] Read as `'b1010`
These bits are fixed with value `'b1010` for all devices in this family.

Bits 11:6 – MJRREV[5:0] Major Revision ID
These bits are used to identify a major revision (A0, B0, C0, etc.).
Revision A = `'b00 0000`
Revision B = `'b00 0001`

Bits 5:0 – MNRREV[5:0] Minor Revision ID
These bits are used to identify a minor revision.
Revision A0 = `'b00 0000`
Revision B0 = `'b00 0000`
Revision B1 = `'b00 0001`

Tip: For example, the REVISIONID register value for revision B1 will be `0xA041`.

3. Programming Algorithms

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state; all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

3.1.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different modes of entering Program/Verify mode via high voltage:

- V_{PP}-First Entry mode
- V_{DD}-First Entry mode

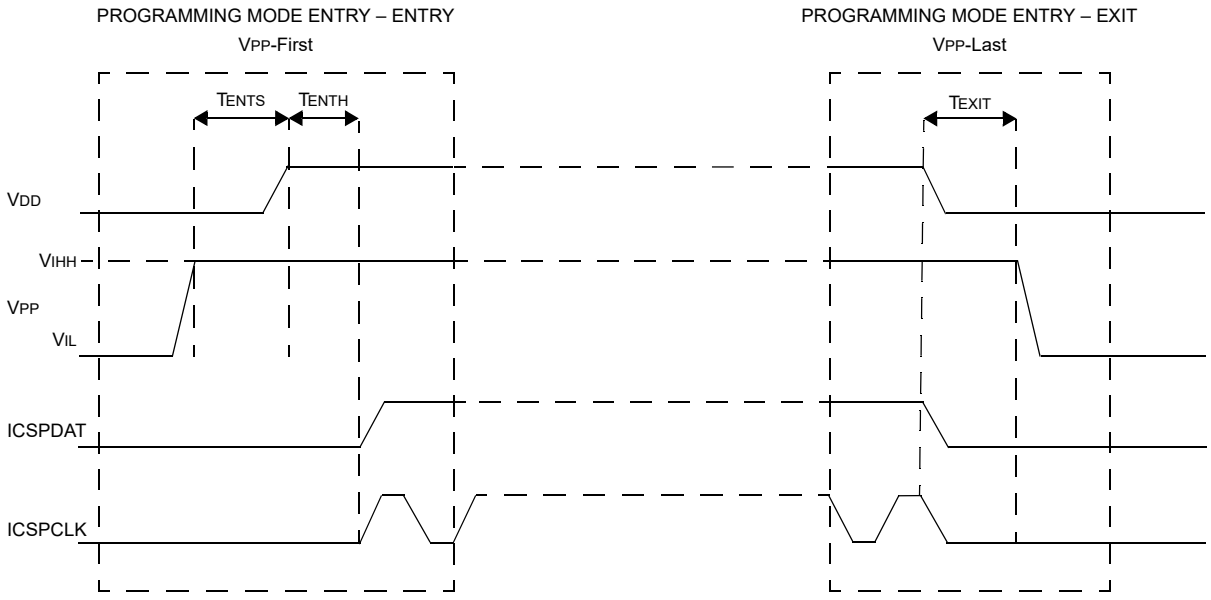
3.1.1.1 V_{PP}-First Entry Mode

To enter Program/Verify mode via the V_{PP}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-First Entry mode prevents the device from executing code prior to entering the Program/Verify mode. For example, when the Configuration Byte has already been programmed to have $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{PWRTE}$ = 0) and the internal oscillator selected, the device will execute the code immediately. V_{PP}-First Entry mode is strongly recommended as it prevents the user code from executing. See the timing diagram in Figure 3-1.

Figure 3-1. Programming Entry and Exit Modes – V_{PP}-First and Last



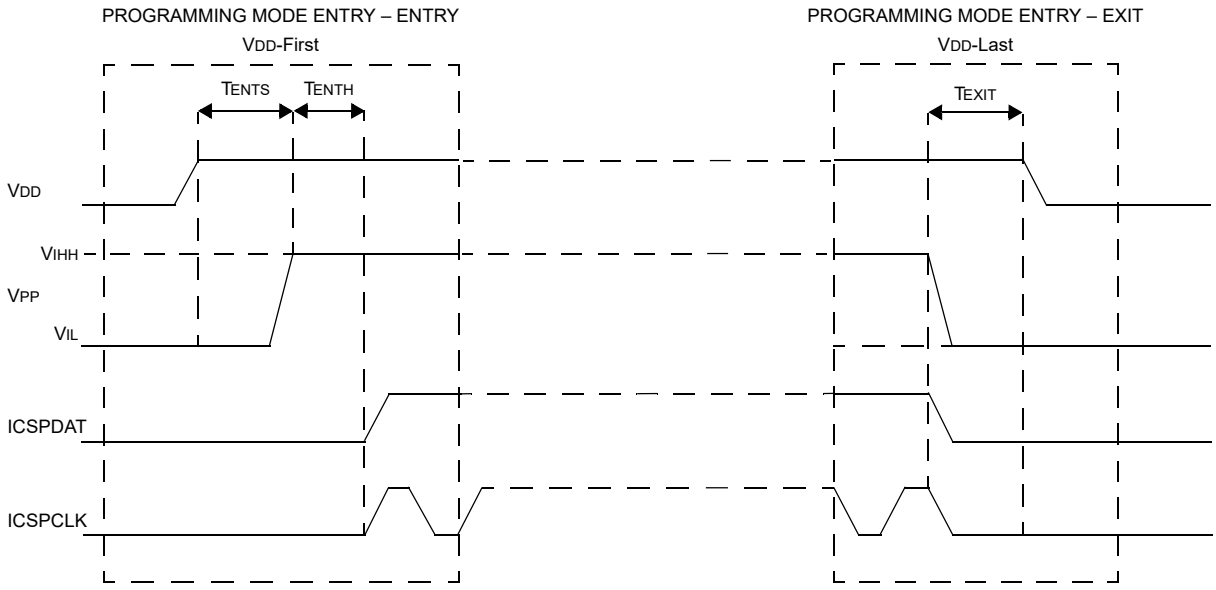
3.1.1.2 V_{DD}-First Entry Mode

To enter the Program/Verify mode via the V_{DD}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-First Entry mode is useful for programming the device when the V_{DD} is already applied. It is not necessary to disconnect V_{DD} to enter the Program/Verify mode. See the timing diagram in Figure 3-2.

Figure 3-2. Programming Entry and Exit Modes – V_{DD}-First and Last



3.1.1.3 Program/Verify Mode Exit

To exit the Program/Verify mode, lower $\overline{MCLR}$ from V_{IHH} to V_{IL}. The V_{PP}-First Entry mode will use the V_{PP}-Last Exit mode (see Figure 3-1). The V_{DD}-First Entry mode will use the V_{DD}-Last Exit mode (see Figure 3-2).

3.1.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit in the Configuration Byte register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, clocked by ICSPCLK. The Least Significant bit (LSb) of the pattern is a 'don't care X'. The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit (MSb) of the Most Significant Byte must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode needs to be maintained. For Low-Voltage Programming timing, see Figure 3-3 and Figure 3-4.

Figure 3-3. LVP Entry (Powered)

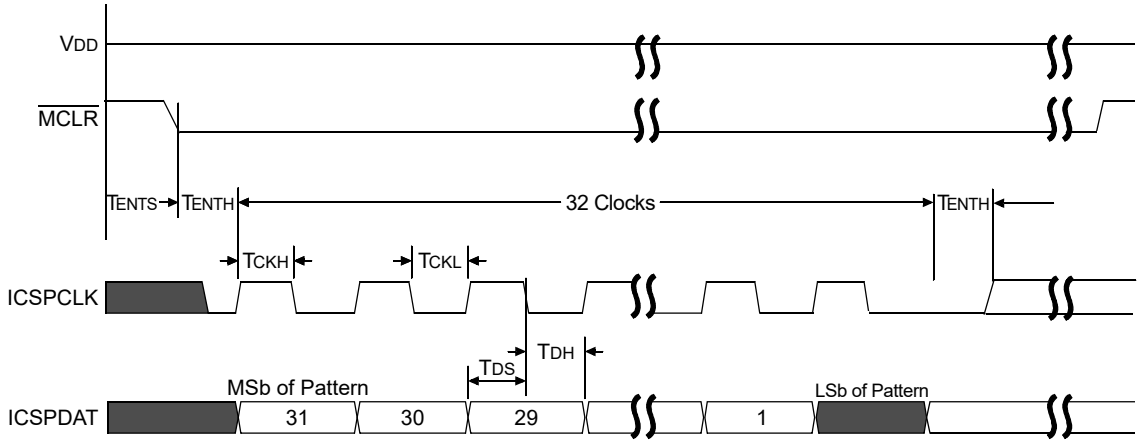
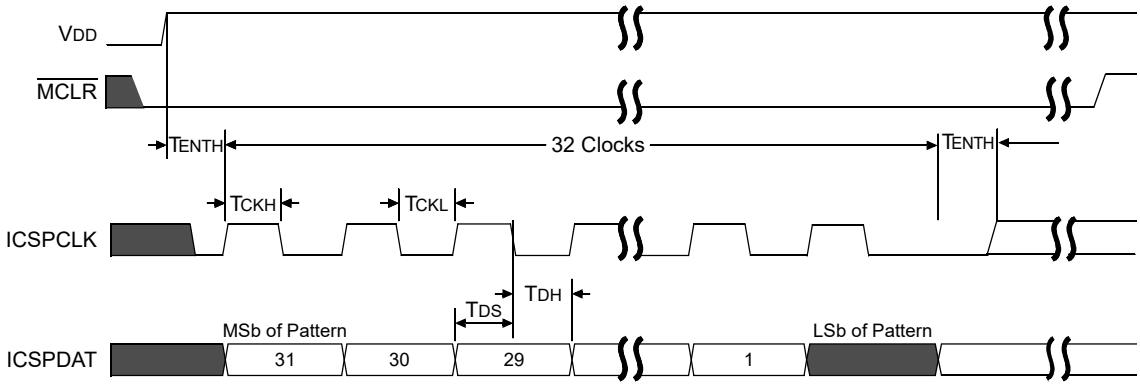


Figure 3-4. LVP Entry (Powering Up)



Exiting the Program/Verify mode is done by raising $\overline{MCLR}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).

Important:
To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

3.1.3 Program/Verify Commands

Once a device has entered the ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue six commands to the microcontroller, each eight bits in length. The commands are summarized in Table 3-1 and are used to erase or program the device based on the location of the Program Counter (PC).

Some 8-bit commands also have an associated data payload (such as Load PC Address and Read Data from NVM).

If the host device issues an 8-bit command byte that has an associated data payload, the host device is responsible for sending additional 24 clock pulses (e.g., three 8-bit bytes) to send or receive the payload data associated with the command.

The payload field size is compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, then by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted MSb first.

When the programming device issues a command that involves a host to the microcontroller payload (e.g., Load PC Address), the Start, Stop and Pad bits will all be driven by the programmer to '0'. When the programming host device

issues a command that involves the microcontroller to host payload data (e.g., Read Data from NVM), the Start, Stop and Pad bits will be treated as 'don't care' bits and the values will be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host will wait a specified minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

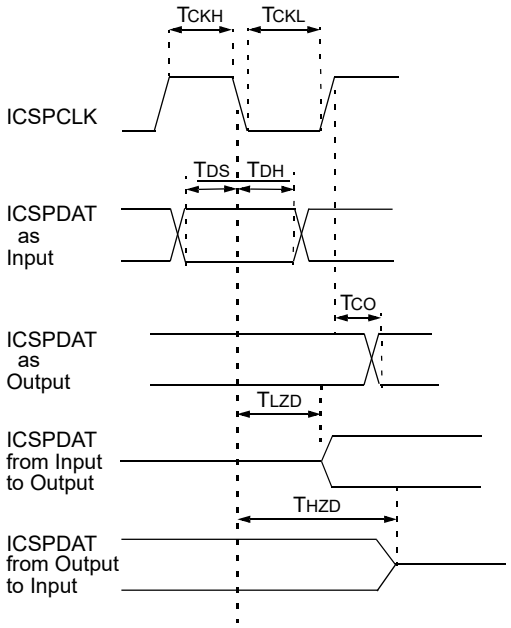
Table 3-1. ICSP™ Command Set Summary(1)

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb ... LSb)	Hex			
Load PC Address	1000 0000	80	Yes	T_{DLY}	Payload value = PC
Bulk Erase	0001 1000	18	Yes	T_{ERAB}	The payload carries the information of the regions that need to be bulk erased
Page Erase Program Memory	1111 0000	F0	No	T_{ERAS}	The page addressed by the MSbs of the PC is erased; LSbs are ignored
Read Data from NVM	1111 11J0	FC/FE	Yes	T_{DLY}	Data output '0' if code-protect is enabled: J = 0: PC is unchanged; J = 1: PC = PC + n(2) after reading
Increment Address	1111 1000	F8	No	T_{DLY}	PC = PC + n(2)
Program Data	11J0 0000	C0/E0	Yes	T_{PROG}	Payload value = Data Word; J = 0: PC is unchanged; J = 1: PC = PC + n after writing

Important:

1. All the clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller will latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and will remain valid for a minimum of T_{DH} after the falling edge of ICSPDAT. See Figure 3-5.
2. PC is incremented by n = 1 for data memory and Configuration Bytes, and n = 2 for all other regions.

Figure 3-5. Clock and Data Timing



3.1.3.1 Program Data

The Program Data command is used to program one NVM word (e.g., one 16-bit instruction word for program memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The payload data are written into program or EEPROM memory immediately after the Programming Data command is issued (see Programming Algorithms). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see Table 3-1).

Figure 3-6. Program Data (Program Memory and User IDs)

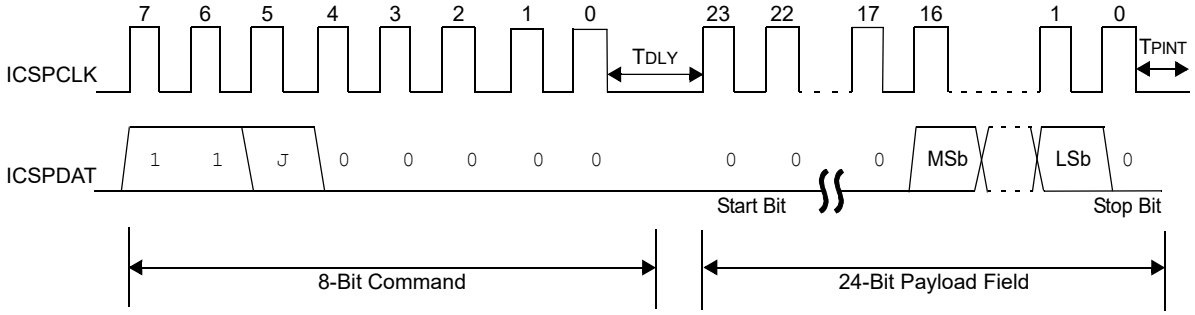
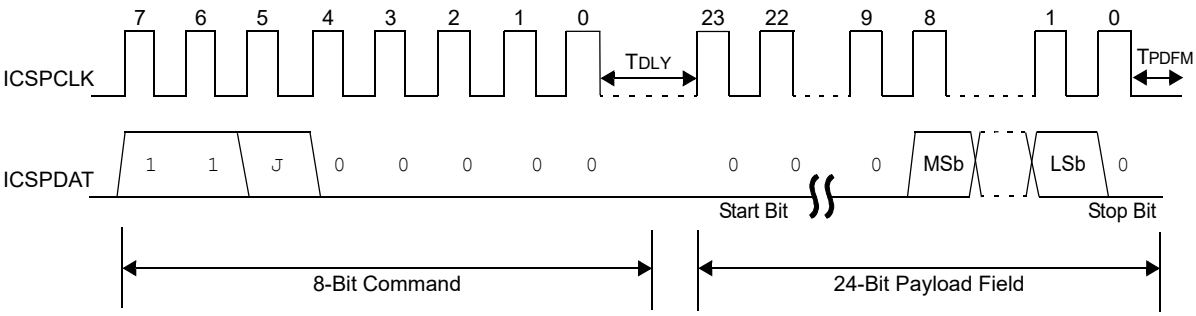


Figure 3-7. Program Data (DATA EEPROM and Configuration Bytes)



3.1.3.2 Read Data from NVM

The Read Data from the NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half of a bit time wide. Therefore, they must be ignored by the host programmer device since the latched value may be indeterminate. Additionally, the host programmer device needs to only consider the MSb to LSb payload bits as valid and can ignore the values of the Pad bits. If the memory region is code-protected ($\overline{CP}$ or $\overline{DP}$), the data will be read as zeros (see Figure 3-8 and Figure 3-9). Depending on the value of bit 1 of the command, the PC may or may not be incremented (see Table 3-1). The Read Data from the NVM command can be used to read data for the Program Flash Memory (see Figure 3-8) or the Data EEPROM Memory (see Figure 3-9).

Figure 3-8. Read Data from NVM (PFM and User IDs)

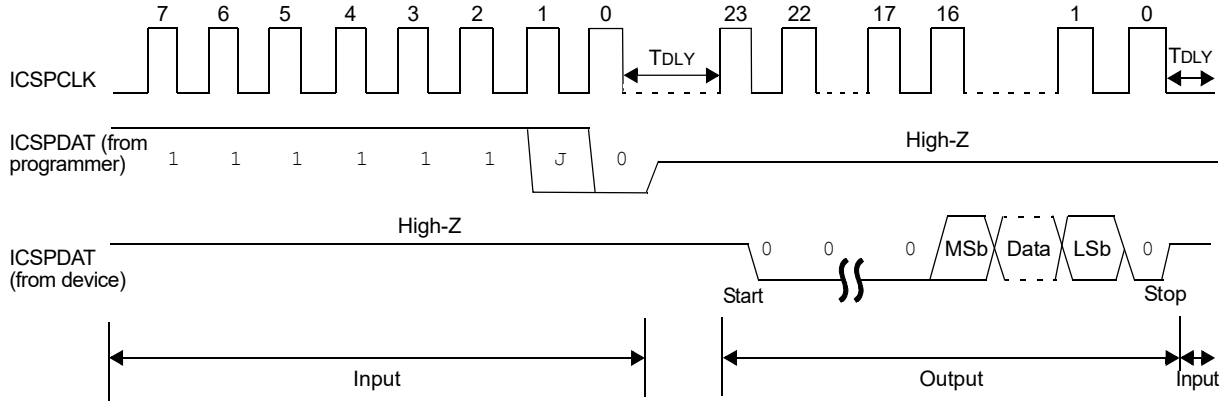
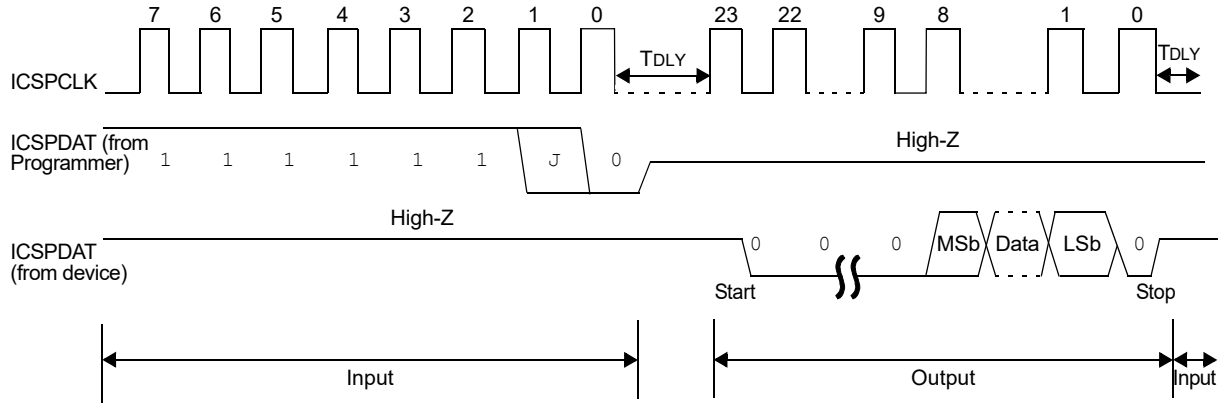


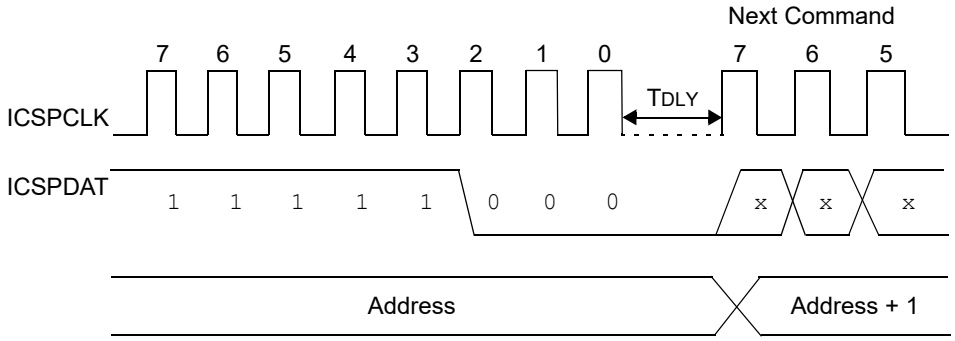
Figure 3-9. Read Data from NVM (DATA EEPROM and Configuration Bytes)



3.1.3.3 Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by 2. If the PC points to the Data EEPROM or Configuration Space, then it is incremented by 1. It is not possible to decrement the address. To reset the Program Counter, the user must use the Load PC Address command.

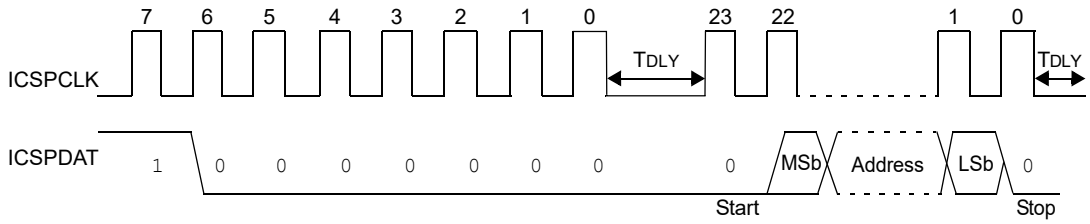
Figure 3-10. Increment Address



3.1.3.4 Load PC Address

The PC value is set using the supplied data. The address indicates the memory location (PFM or Data EEPROM Memory or Configuration memory) to be accessed (see Figure 3-11).

Figure 3-11. Load PC Address



3.1.3.5 Bulk Erase

The Bulk Erase command is used to completely erase different memory regions. The area selection is a bit field in the payload.

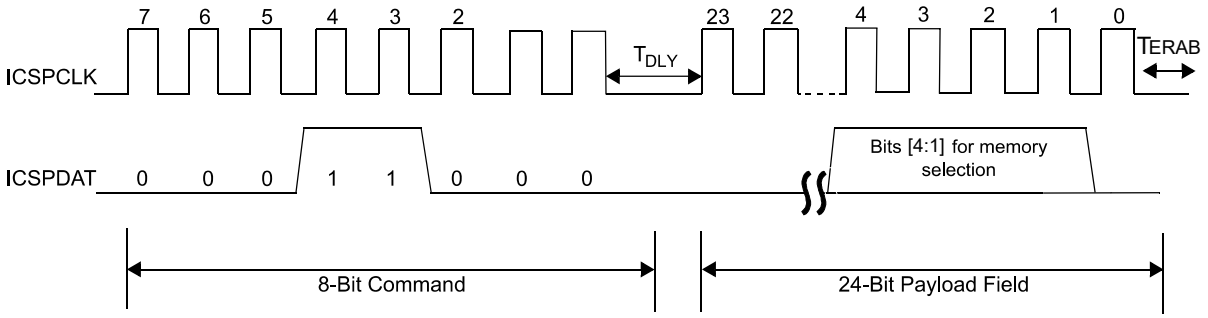
By setting the following bits of the payload, the corresponding memory regions can be bulk erased. Setting multiple bits is valid.

1. Bit 0: Data EEPROM
2. Bit 1: Flash memory
3. Bit 2: User ID memory
4. Bit 3: Configuration memory

Important: If the device is code-protected and a Bulk Erase command for the Configuration memory is issued, all other regions are also bulk erased.

After receiving the Bulk Erase command, the erase will complete after the time interval, T_{ERAB}. See Figure 3-12 for the Bulk Erase command structure.

Figure 3-12. Bulk Erase Memory

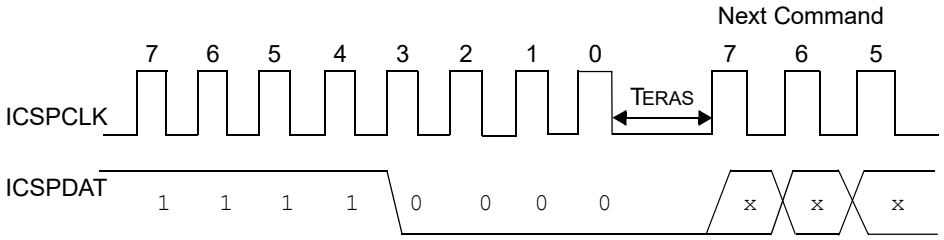


3.1.3.6 Page Erase Program Memory

The Page Erase Program Memory command will erase an individual page based on the current address of the Program Counter. If the program memory is code-protected, the Page Erase Memory command will be ignored. The Bulk Erase command must be used to erase code-protected memory.

The Flash memory page defined by the current PC will be erased. The user must wait T_{ERAS} for erasing to be complete (see Figure 3-13). Page Erase may be used for the program memory and User ID regions only. The configuration and data regions must be erased with the Bulk Erase method.

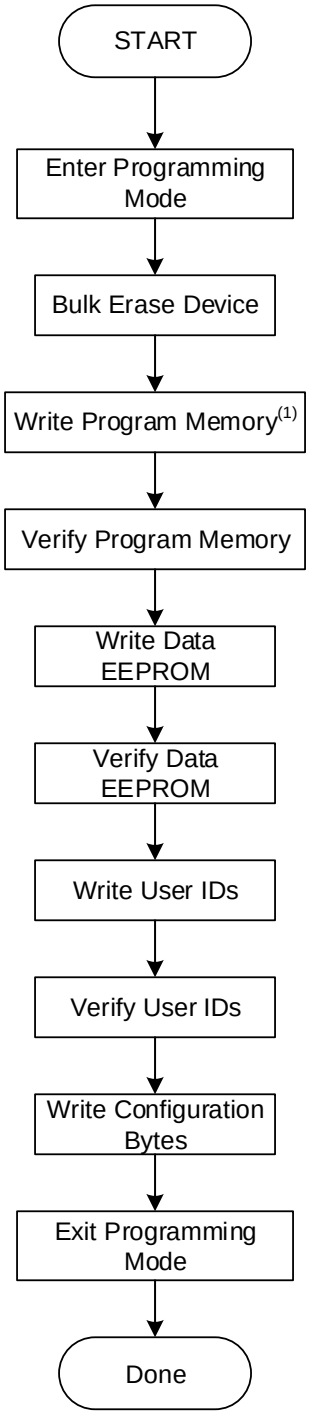
Figure 3-13. Page Erase Memory



3.2 Programming Algorithms

The Program Flash Memory and User ID are programmed one word at a time. The EEPROM memory and configuration regions are programmed one byte at a time.

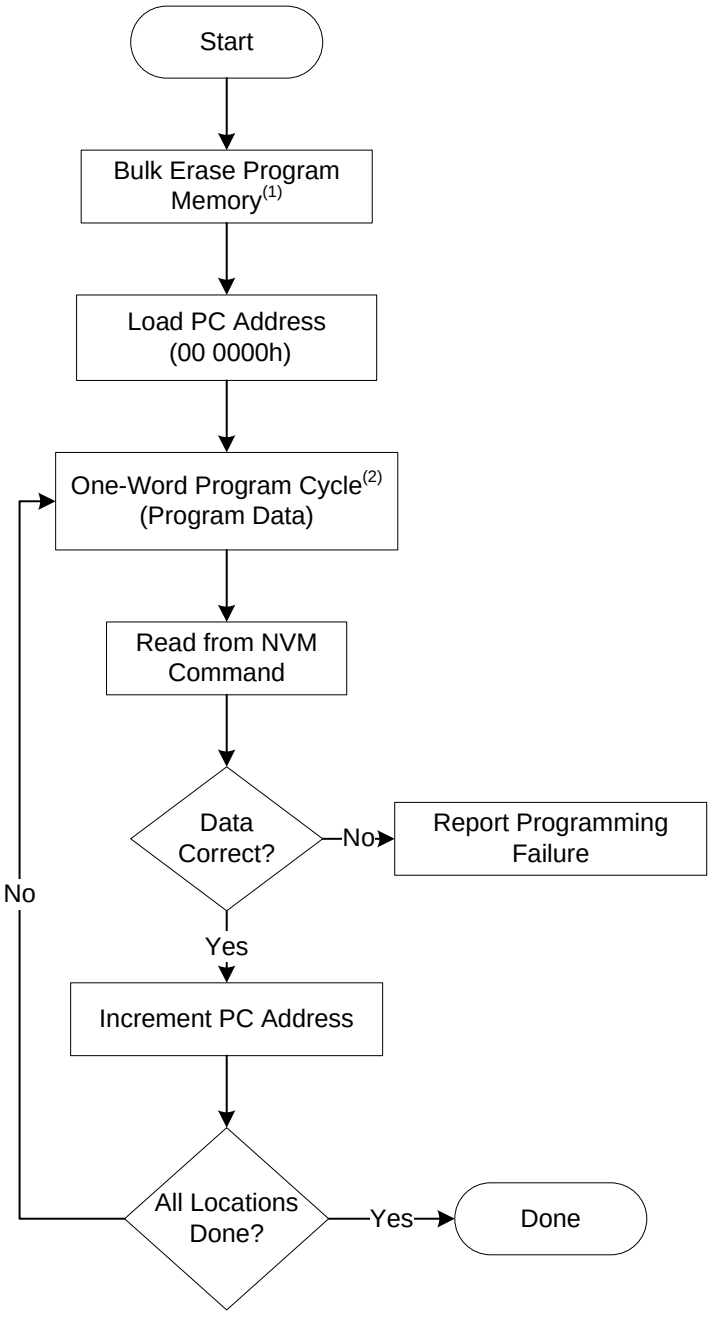
Figure 3-14. Device Program/Verify Flowchart



Notes:

1. See Figure 3-15.
2. See Figure 3-17.

Figure 3-15. Program Memory Flowchart



Notes:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device, as shown in Figure 3-18.

Figure 3-16. One-Word Program Cycle

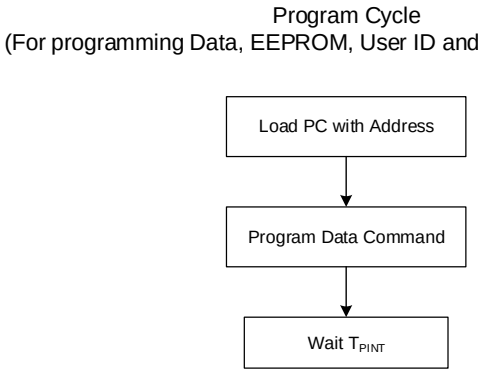
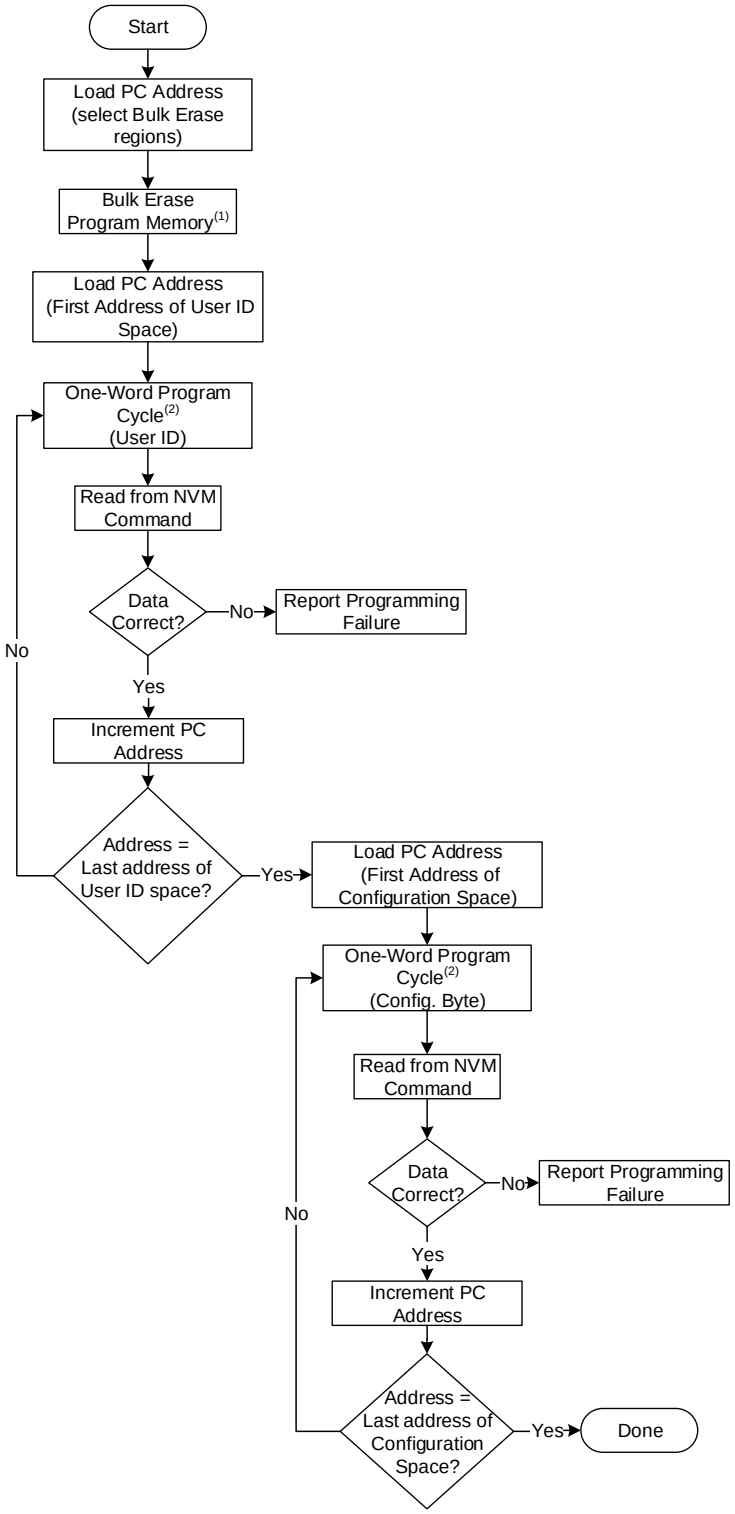


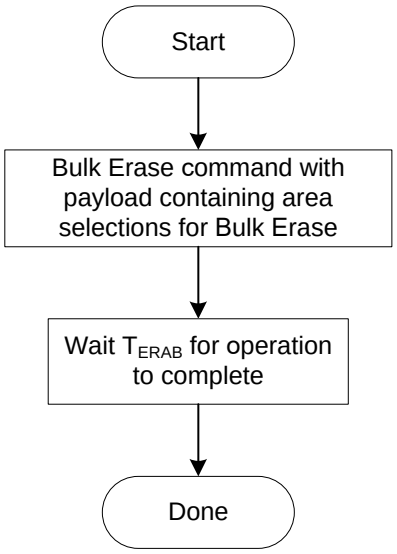
Figure 3-17. User ID and Configuration Memory Program Flowchart



Notes:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. See Figure 3-16.

Figure 3-18. Bulk Erase Flowchart



3.3 Code Protection

Code protection is controlled using the $\overline{CP}$ bit. When code protection is enabled, all program memory and Data EEPROM locations read as '0'. Further programming is disabled for the program memory and Data EEPROM until a Bulk Erase operation is performed on the configuration memory region. The program memory and Data EEPROM can still be programmed and read during program execution.

The User ID locations and Configuration Bytes can be programmed and read out regardless of the code protection settings.

The only way to disable code protection is to use the Bulk Erase Program Memory command with bit 4 of the payload set to '1'. This will clear the disable code protection and erase all memory locations.

3.4 Hex File Usage

3.4.1 Embedding Configuration Information in the Hex File

To allow the portability of the code, a programmer is required to read the Configuration Byte locations from the hex file. If the Configuration Byte information is not present in the hex file, then a simple warning message will be issued. Similarly, when saving a hex file, all the Configuration Byte information will be included. An option not to include the Configuration Byte information may be provided. When embedding Configuration Byte information in the hex file, it will start at address 30 0000h.

Important:
This feature is highly important for the benefit of the end customer.

3.4.2 Embedding Data EEPROM Information in the Hex File

To allow the portability of the code, a programmer is required to read the Data EEPROM information from the hex file. If Data EEPROM information is not present, a simple warning message will be issued. Similarly, when saving a hex file, all Data EEPROM information must be included. An option not to include the Data EEPROM information may be provided. When embedding Data EEPROM information in the hex file, it will start at address 38 0000h.

Important:
This feature is highly important for the benefit of the end customer.

3.5 CRC Checksum Computation

Unlike older PIC® devices, the Microchip toolchain runs a 32-bit CRC calculation on the entire hex file to calculate its checksum. The checksum uses the standard CRC-32 algorithm with the polynomial 0x4C11DB7 $\left(x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1\right)$.

4. Electrical Specifications

Refer to the device specific data sheet for absolute maximum ratings.

Table 4-1. AC/DC Characteristics Timing Requirements for Program/Verify Mode

AC/DC Characteristics		Standard Operating Conditions Production Tested at +25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/ Comments**
Programming Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	1.80	—	5.50	V	**(Note 1)**
V_{PEW}	Read/Write and Page Erase Operations	V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase Operations	V_{BORMAX}	—	V_{DDMAX}	V	**(Note 2)**
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	10	mA	
I_{PP}	**V_{PP}**					
	Current on $\overline{MCLR}/V_{PP}$	—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify Mode Entry	7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/ Verify Mode Entry	—	—	1.0	µs	
V_{IH}	**I/O Pins**					
	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input High Level	0.8 V_{DD}	—	V_{DD}	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input Low Level	V_{SS}	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level	V_{DD} – 0.7	—	—	V	I_{OH} = 3 mA, V_{DD} = 3.0V
V_{OL}	ICSPDAT Output Low Level	—	—	V_{SS} + 0.6	V	I_{OL} = 6 mA, V_{DD} = 3.0V
Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time before V_{DD} or $\overline{MCLR}$↑	1	—	—	ms	
Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in Setup Time before Clock↓	100	—	—	ns	
T_{DH}	Data in Hold Time after Clock↓	100	—	—	ns	
T_{CO}	Clock↑ to Data Out Valid (during a Read Data command)	0	—	80	ns	

.....continued

AC/DC Characteristics		Standard Operating Conditions Production Tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/ Comments
T_{LZD}	Clock↓ to Data Low-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{HZD}	Clock↓ to Data High-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{DLY}	Data Input not Driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase Cycle Time	—	—	11	ms	Program, Config and ID
T_{ERAS}	Page Erase Cycle Time	—	—	11	ms	
T_{PDFM}	Internally Timed DFM (EEPROM) Programming Operation Time	—	—	11	ms	EEPROM and Configuration Bytes
T_{PINT}	Internally Timed Programming Operation Time	—	—	75	µs	Program Memory and User IDs
T_{EXIT}	Time Delay when Exiting Program/Verify Mode	1	—	—	µs	

Notes:

1. Bulk erased devices default to Brown-out Reset enabled with BORV = `11` (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = `1`) when performing Low-Voltage Programming on a bulk erased device to ensure that the device is not held in Brown-out Reset.
2. The hardware requires V_{DD} to be above the BOR threshold, at the ~2.85V nominal setting, to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the V_{BOR} level.

5. Appendix A: Revision History

Doc Rev.	Date	Comments
D	07/2021	Updated Table 4-1 and Sections 2.6, 3.1.2, 3.1.3.5, 6.3 and 6.5. Changed *Configuration Words* to *Configuration Bytes*. Minor editorial corrections.
C	09/2020	Updated Table 6-2 and Section 2.5; other minor corrections
B	10/2019	Updated Table 4-1 - T_{PINT} from 50 µs to 75 µs
A	07/2019	Initial document release

6. Appendix B

This section provides information about the device IDs and pinout descriptions.

Table 6-1. Programming Pin Locations by Package Type

Device	Package	Package Code	V_{DD}	V_{SS}	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
			PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC18F26Q83 PIC18F26Q84 PIC18F27Q83 PIC18F27Q84	28-Pin SPDIP	(SP)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin SOIC	(SO)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin SSOP	(SS)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin VQFN	(5N)	17	16, 5	26	RE3	24	RB6	25	RB7
PIC18F46Q83 PIC18F46Q84 PIC18F47Q83 PIC18F47Q84	40-Pin PDIP	(P)	32, 11	31, 12	1	RE3	39	RB6	40	RB7
	40-Pin VQFN	(NHX)	26, 7	27, 6	16	RE3	14	RB6	15	RB7
	44-Pin TQFP	(PT)	28, 7	29, 6	18	RE3	16	RB6	17	RB7
PIC18F56Q83 PIC18F56Q84 PIC18F57Q83 PIC18F57Q84	48-Pin TQFP	(PT)	30, 7	31 , 6	20	RE3	18	RB6	19	RB7
	48-Pin VQFN	(6MX)	30, 7	31, 6	20	RE3	18	RB6	19	RB7

Note:
The most current package drawings are located in the Microchip Packaging Specification, DS00000049 (http://www.microchip.com/packaging). The drawing numbers listed above do not include the current revision designator, which is added at the end of the number.

6.1 CONFIG1

Name: CONFIG1
Offset: 30 0000h

Configuration Byte 1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	1		1	1	1

Bits 6:4 – RSTOSC[2:0] Power-Up Default Value for COSC
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1. Resets COSC/NOSC to b'110'.
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
001	Reserved
000	HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1. Resets COSC/NOSC to b'110'.

Bits 2:0 – FEXTOSC[2:0] External Oscillator Mode Selection

Value	Description
111	ECH (external clock) above 8 MHz
110	ECM (external clock) for 500 kHz to 8 MHz
101	ECL (external clock) below 500 kHz
100	Oscillator not enabled
011	Reserved (do not use)
010	HS (crystal oscillator) above 4 MHz
001	XT (crystal oscillator) above 500 kHz, below 4 MHz
000	LP (crystal oscillator) optimized for 32.768 kHz

6.2 CONFIG2

Name: CONFIG2
Offset: 30 0001h

Configuration Byte 2

Bit	7	6	5	4	3	2	1	0
	FCMENS	FCMENP	FCMEN	JTAGEN	CSWEN		PR1WAY	$\overline{\text{CLKOUTEN}}$
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	1	1	1	1	1		1	1

Bit 7 – FCMENS Fail-Safe Clock Monitor Enable for Secondary Crystal Oscillator Enable

Value	Description
1	Fail-Safe Clock Monitor enabled for Secondary Crystal; Fail-Safe timer will set the FSCMS bit and trigger OSFIF interrupt on secondary crystal failure
0	Fail-Safe Clock Monitor disabled for Secondary Crystal

Bit 6 – FCMENP Fail-Safe Clock Monitor Enable for Primary Crystal Oscillator

Value	Description
1	Fail-Safe Clock Monitor enabled for Primary Crystal Oscillator; Fail-Safe timer will set FSCMP bit and trigger OSFIF interrupt on primary crystal failure
0	Fail-Safe Clock Monitor disabled for Primary Crystal Oscillator

Bit 5 – FCMEN Fail-Safe Clock Monitor Enable for FOSC

Value	Description
1	Fail-Safe Clock Monitor enabled; Fail-Safe timer will initiate a clock switch and trigger OSFIF interrupt on FOSC failure
0	Fail-Safe Clock Monitor disabled

Bit 4 – JTAGEN JTAG Boundary Scan Enable

Value	Description
1	Enable JTAG Boundary Scan mode and pins
0	Disable JTAG Boundary Scan mode, JTAG pins revert to user functions

Bit 3 – CSWEN Clock Switch Enable

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 1 – PR1WAY PRLOCKED One-Way Set Enable

Value	Description
1	The PRLOCKED bit can be cleared and set only once; Priority registers remain locked after one clear/set cycle
0	The PRLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 0 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable
If FEXTOSC = HS, XT, LP, then this bit is ignored.
Otherwise:

Value	Description
1	CLKOUT function is disabled; I/O function on OSC2
0	CLKOUT function is enabled; $F_{OSC}/4$ clock appears at OSC2

6.3 CONFIG3

Name: CONFIG3
Offset: 30 0002h

Configuration Byte 3

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]		$\overline{\text{LPBOREN}}$	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	1	1

Bits 7:6 – BOREN[1:0] Brown-out Reset Enable
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit.

Value	Description
11	Brown-out Reset enabled, the SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – $\overline{\text{LPBOREN}}$ Low-Power BOR Enable

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bit 4 – IVT1WAY IVTLOCK One-Way Set Enable

Value	Description
1	The IVTLOCK bit can be cleared and set only once; IVT registers remain locked after one clear/set cycle
0	The IVTLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 3 – MVECEN Multivector Enable

Value	Description
1	Multivector is enabled; vector table used for interrupts
0	Legacy interrupt behavior

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection

Value	Description
11	PWRT is disabled
10	PWRT is set at 64 ms
01	PWRT is set at 16 ms
00	PWRT is set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable

Value	Condition	Description
x	If LVP = 1	RE3 pin function is $\overline{\text{MCLR}}$
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is a port-defined function

6.4 CONFIG4

Name: CONFIG4
Offset: 30 0003h

Configuration Byte 4

Bit	7	6	5	4	3	2	1	0
	$\overline{XINST}$		LVP	STVREN	PPS1WAY	$\overline{ZCD}$	BORV[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	1		1	1	1	1	1	1

Bit 7 – $\overline{XINST}$ Extended Instruction Set Enable

Value	Description
1	Extended Instruction Set and Indexed Addressing mode disabled (Legacy mode)
0	Extended Instruction Set and Indexed Addressing mode enabled

Bit 5 – LVP Low-Voltage Programming Enable
The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

Value	Description
1	Low-Voltage Programming enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. The MCLRE Configuration bit is ignored.
0	HV on $\overline{MCLR}/V_{PP}$ must be used for programming

Bit 4 – STVREN Stack Overflow/Underflow Reset Enable

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 3 – PPS1WAY PPSLOCKED One-Way Set Enable

Value	Description
1	The PPSLOCKED bit can only be set once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
0	The PPSLOCKED bit can be set and cleared as needed (unlocking sequence is required)

Bit 2 – $\overline{ZCD}$ ZCD Disable

Value	Description
1	ZCD disabled, ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
0	ZCD always enabled, PMDx[ZCDMD] bit is ignored

Bits 1:0 – BORV[1:0] Brown-out Reset Voltage Selection(1)

Value	Description
11	Brown-out Reset Voltage (V_{BOR}) set to 1.90V
10	Brown-out Reset Voltage (V_{BOR}) set to 2.45V
01	Brown-out Reset Voltage (V_{BOR}) set to 2.7V
00	Brown-out Reset Voltage (V_{BOR}) set to 2.85V

Note:

1. The higher voltage setting is recommended for an operation at or above 16 MHz.

6.5 CONFIG5

Name: CONFIG5
Offset: 30 0004h

Configuration Byte 5

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	1	1	1	1	1

Bits 6:5 – WDTE[1:0] WDT Operating Mode

Value	Description
11	WDT enabled regardless of Sleep; the SEN bit in WDTCON0 is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; the SEN bit in WDTCON0 is ignored
01	WDT enabled/disabled by the SEN bit in WDTCON0
00	WDT disabled, the SEN bit in WDTCON0 is ignored

Bits 4:0 – WDTCPS[4:0] WDT Period Select

WDTCPS	WDTCON0[WDTPS] at POR				Software Control of WDTPS?
	Value	Divider Ratio		Typical Time Out (F_{IN} = 31 kHz)	
11111	01011	1:65536	2^{16}	2s	Yes
11110 to 10011	11110 to 10011	1:32	2^{5}	1 ms	No
10010	10010	1:8388608	2^{23}	256s	No
10001	10001	1:4194304	2^{22}	128s	No
10000	10000	1:2097152	2^{21}	64s	No
01111	01111	1:1048576	2^{20}	32s	No
01110	01110	1:524288	2^{19}	16s	No
01101	01101	1:262144	2^{18}	8s	No
01100	01100	1:131072	2^{17}	4s	No
01011	01011	1:65536	2^{16}	2s	No
01010	01010	1:32768	2^{15}	1s	No
01001	01001	1:16384	2^{14}	512 ms	No
01000	01000	1:8192	2^{13}	256 ms	No
00111	00111	1:4096	2^{12}	128 ms	No
00110	00110	1:2048	2^{11}	64 ms	No
00101	00101	1:1024	2^{10}	32 ms	No
00100	00100	1:512	2^{9}	16 ms	No
00011	00011	1:256	2^{8}	8 ms	No
00010	00010	1:128	2^{7}	4 ms	No
00001	00001	1:64	2^{6}	2 ms	No
00000	00000	1:32	2^{5}	1 ms	No

6.6 CONFIG6

Name: CONFIG6
Offset: 30 0005h

Configuration Byte 6

Bit	7	6	5	4	3	2	1	0
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:3 – WDTCCS[2:0] WDT Input Clock Selector

Value	Condition	Description
x	WDTE = 00	These bits have no effect
111	WDTE ≠ 00	Software control
110 to 011	WDTE ≠ 00	Reserved
010	WDTE ≠ 00	WDT reference clock is the SOSC
001	WDTE ≠ 00	WDT reference clock is the 31.25 kHz MFINTOSC
000	WDTE ≠ 00	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 2:0 – WDTCWS[2:0] WDT Window Select

WDTCWS	WDTCON1[WINDOW] at POR			Software Control of WINDOW	Keyed Access Required?
	Value	Window Delay Percent of Time	Window Opening Percent of Time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

6.7 CONFIG7

Name: CONFIG7
Offset: 30 0006h

Configuration Byte 7

Bit	7	6	5	4	3	2	1	0
			$\overline{\text{DEBUG}}$	$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit 5 – $\overline{\text{DEBUG}}$ Debugger Enable

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 4 – $\overline{\text{SAFEN}}$ Storage Area Flash (SAF) Enable(1)

Value	Description
1	SAF is disabled
0	SAF is enabled

Bit 3 – $\overline{\text{BBEN}}$ Boot Block Enable(1)

Value	Description
1	Boot Block is disabled
0	Boot Block is enabled

Bits 2:0 – BBSIZE[2:0] Boot Block Size Selection(2)

Table 6-2. Boot Block Size

$\overline{\text{BBEN}}$	BBSIZE	End Address of Boot Block	Boot Block Size (words)	
			PIC18Fx6Q83/Q84	PIC18Fx7Q83/Q84
1	xxx	–	–	
0	111	00 03FFh	512	
0	110	00 07FFh	1024	
0	101	00 0FFFh	2048	
0	100	00 1FFFh	4096	
0	011	00 3FFFh	8192	
0	010	00 7FFFh	16384	
0	001	00 FFFFh	–	32768
0	000	01 FFFFh	–	

Notes:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. BBSIZE[2:0] bits can only be changed when BBEN = 1. Once BBEN = 0, BBSIZE[2:0] can only be changed through a Bulk Erase.

6.8 CONFIG8

Name: CONFIG8
Offset: 30 0007h

Configuration Byte 8

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$				$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access	R/W				R/W	R/W	R/W	R/W
Reset	1				1	1	1	1

Bit 7 – $\overline{\text{WRTAPP}}$ Application Block Write Protection(1)

Value	Description
1	Application Block is not write-protected
0	Application Block is write-protected

Bit 3 – $\overline{\text{WRTSAF}}$ Storage Area Flash (SAF) Write Protection(1,2)

Value	Description
1	SAF is not write-protected
0	SAF is write-protected

Bit 2 – $\overline{\text{WRTD}}$ Data EEPROM Write Protection(1)

Value	Description
1	Data EEPROM is not write-protected
0	Data EEPROM is write-protected

Bit 1 – $\overline{\text{WRTC}}$ Configuration Register Write Protection(1)

Value	Description
1	Configuration registers are not write-protected
0	Configuration registers are write-protected

Bit 0 – $\overline{\text{WRTB}}$ Boot Block Write Protection(1,3)

Value	Description
1	Boot Block is not write-protected
0	Boot Block is write-protected

Notes:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. Applicable only if $\overline{\text{SAFEN}}$ = 0.
3. Applicable only if $\overline{\text{BBEN}}$ = 0.

6.9 CONFIG9

Name: CONFIG9
Offset: 30 0008h

Configuration Byte 9

Bit	7	6	5	4	3	2	1	0
			$\overline{\text{ODCON}}$	$\overline{\text{BPEN}}$			BOOTPINSEL[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	1			1	1

Bit 5 – $\overline{\text{ODCON}}$ CRC-on-Boot Pin Open-Drain Configuration

Value	Description
1	CRC-on-boot output drives both high-going and low-going signals (source and sink current)
0	CRC-on-boot output drives only low-going signals (sink current only)

Bit 4 – $\overline{\text{BPEN}}$ CRC-on-Boot Output Pin Enable

Value	Description
1	CRC-on-boot output pin disabled
0	CRC-on-boot output pin determined by BOOTPINSEL[1:0]

Bits 1:0 – BOOTPINSEL[1:0] CRC-on-Boot Pin Select

Value	Description
11	CRC-on-boot output pin is RC5
10	CRC-on-boot output pin is RC4
01	CRC-on-boot output pin is RA2
00	CRC-on-boot output pin is RA4

6.10 CONFIG10

Name: CONFIG10
Offset: 30 0009h

Configuration Byte 10

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access								R/W
Reset								1

Bit 0 – $\overline{CP}$ User Program Flash Memory and Data EEPROM Code Protection(1)

Value	Description
1	User Program Flash Memory and Data EEPROM code protection are disabled
0	User Program Flash Memory and Data EEPROM code protection are enabled

Note:

1. Once this bit is enabled, it can only be reset through a Bulk Erase.

6.11 CONFIG11

Name: CONFIG11
Offset: 30 000Ah

Configuration Byte 11

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{BOOTPOR}}$	$\overline{\text{COE}}$	$\overline{\text{CFGSCEN}}$	$\overline{\text{DATSCEN}}$	$\overline{\text{SAFSCEN}}$	$\overline{\text{APPSCEN}}$	$\overline{\text{BOOTCOE}}$	$\overline{\text{BOOTSCEN}}$
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 7 – $\overline{\text{BOOTPOR}}$ CRC-on-Boot Enable

Value	Description
1	CRC-on-boot disabled, device will immediately execute user code upon device Reset
0	CRC-on-boot enabled, device will perform CRC check of configured memory before executing user code upon device Reset

Bit 6 – $\overline{\text{COE}}$ Continue on Error for Non-Boot Block Areas Enable

Value	Description
1	Device will halt if a mismatch is found between expected and calculated CRC values for the non-boot block areas of memory
0	Device will continue execution even if a mismatch is found between expected and calculated CRC values for the non-boot block areas of memory

Bit 5 – $\overline{\text{CFGSCEN}}$ Non-Boot Block Area CRC Configuration Fuse Scan Enable

Value	Description
1	Non-boot block area CRC scan/calculation will not include Configuration Fuse values in its calculation
0	Non-boot block area CRC scan/calculation will include all Configuration Fuse values except CONFIG14H-CONFIG16L in its calculation

Bit 4 – $\overline{\text{DATSCEN}}$ Non-Boot Block Area CRC Data EEPROM Scan Enable

Value	Description
1	Non-boot block area CRC scan/calculation will not include Data EEPROM values in its calculation
0	Non-boot block area CRC scan/calculation will include Data EEPROM values in its calculation

Bit 3 – $\overline{\text{SAFSCEN}}$ Non-Boot Block Area CRC SAF Area Scan Enable

Value	Description
1	Non-boot block area CRC scan/calculation will not include SAF area of Flash memory in its calculation if SAF area is enabled
0	Non-boot block area CRC scan/calculation will include SAF area of Flash memory in its calculation if SAF area is enabled

Bit 2 – $\overline{\text{APPSCEN}}$ Non-Boot Block Area CRC Application Code Area Scan Enable

Value	Description
1	Non-boot block area CRC scan/calculation will not include main application code area of Flash memory in its calculations
0	Non-boot block area CRC scan/calculation will include main application code area of Flash memory in its calculations

Bit 1 – $\overline{\text{BOOTCOE}}$ Continue on Error for Boot Block Areas Enable

Value	Description
1	Device will halt if a mismatch is found between expected and calculated CRC values for the boot block areas of memory
0	Device will continue execution even if a mismatch is found between expected and calculated CRC values for the boot block areas of memory

Bit 0 – $\overline{\text{BOOTSCEN}}$ Boot Block Area CRC Scan Enable

Value	Description
1	CRC Scan/calculation on boot block area will not be run
0	CRC Scan/calculation on boot block area will be run

6.12 CRC Boot Polynomial

Name: CRC Boot Polynomial
Offset: 30 000Bh

The Polynomial for the CRC of the boot block segment of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the polynomial configuration spans from CONFIG12 to CONFIG15, with the MSB of CONFIG12 being the XOR of polynomial term X^{31} and the LSB of CONFIG15 being the XOR of polynomial term X^0.

Bit	31	30	29	28	27	26	25	24
	BCRCPOL[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	BCRCPOL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	BCRCPOL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BCRCPOL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – BCRCPOL[31:0] XOR of Polynomial Term X^n Enable bits

6.13 CRC Boot Seed

Name: CRC Boot Seed
Offset: 30 000Fh

The Seed for the CRC of the boot block segment of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the boot block seed spans from CONFIG16 to CONFIG19, with the MSB of CONFIG16 being the MSB of the seed and the LSB of CONFIG19 being the LSB of the seed.

Bit	31	30	29	28	27	26	25	24
	BCRCSEED[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	BCRCSEED[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	BCRCSEED[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BCRCSEED[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – BCRCSEED[31:0] Boot Block CRC Seed Field

6.14 CRC Boot Expected Value

Name: CRC Boot Expected Value
Offset: 30 0013h

The Expected Value for the CRC of the boot block segment of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the expected value spans from CONFIG20 to CONFIG23, with the MSB of CONFIG20 being the MSB of the expected value, and the LSB of CONFIG23 being the LSB of the expected value.

Bit	31	30	29	28	27	26	25	24
	BCRCERES[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	BCRCERES[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	BCRCERES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BCRCERES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – BCRCERES[31:0] Boot Block Area CRC Expected Result

6.15 CRC Polynomial

Name: CRC Polynomial
Offset: 30 0017h

The Polynomial for the CRC of the non-boot block segments of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the polynomial configuration spans from CONFIG24 to CONFIG27, with the MSB of CONFIG24 being the XOR of polynomial term X^{31} and the LSB of CONFIG27 being the XOR of polynomial term X^0.

Bit	31	30	29	28	27	26	25	24
	CRCPOL[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	CRCPOL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	CRCPOL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	CRCPOL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – CRCPOL[31:0] XOR of Polynomial Term X^n Enable bits

6.16 CRC Seed

Name: CRC Seed
Offset: 30 001B

The Seed for the CRC of the non-boot block segments of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the seed spans from CONFIG28 to CONFIG31, with the MSB of CONFIG28 being the MSB of the seed and the LSB of CONFIG31 being the LSB of the seed.

Bit	31	30	29	28	27	26	25	24
	CRCSEED[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	CRCSEED[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	CRCSEED[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	CRCSEED[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – CRCSEED[31:0] Non-Boot Block Area CRC Seed Field

6.17 CRC Expected Value

Name: CRC Expected Value
Offset: 30 001F

The Expected Value for the CRC of the non-boot block segments of memory
Note: The CRC-on-boot module uses a 32-bit polynomial, as such the expected value spans from CONFIG32 to CONFIG35, with the MSB of CONFIG32 being the MSB of the expected value, and the LSB of CONFIG35 being the LSB of the expected value.

Bit	31	30	29	28	27	26	25	24
	CRCERES[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	CRCERES[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	CRCERES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	CRCERES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – CRCERES[31:0] Non-Boot Block Area CRC Expected Result

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