MXTAN0208

Design Guidelines for PCB Layouts for maXTouch Controllers

TABLE OF CONTENTS

1.0 Introduction 2
2.0 Initial Preparation 3
3.0 Trace Routing 4
- 3.1 Signal Tracking 4
- 3.2 Track Width Rules 4
- 3.3 Board Layers 4
- 3.4 Y Lines 4
- 3.5 X Lines 5
- 3.6 Guard Track (Self Capacitance Measurements) 6
- 3.7 Shielding and Ground 6
- 3.8 ESD Ground Routing 6
- 3.9 Power Traces 7
- 3.10 Vdd 7
- 3.11 AVdd 8
- 3.12 XVdd 8
- 3.13 VddCORE 8
- 3.14 Ground 8
- 3.15 Low Drop-out Voltage Regulators 10

4.0 Communication Traces 12
- 4.1 SPI Traces 12
- 4.2 I2C Traces 12
- 4.3 Crystal Selection 12
- 4.4 Other Traces 12
- 4.5 ESD Handling 13

5.0 External High Voltage Circuit Layout 14
6.0 BGA Escape Routing 15
7.0 Design for Manufacturing 16
- 7.1 Layout Traces 16
- 7.2 Vias 16
- 7.3 Solder Mask 16
- 7.4 Layer Stack-up 17

8.0 Flexible Printed Circuit 18
- 8.1 FPC Layout 18
- 8.2 FPC Orientation 19
- 8.3 FPC Folding Path 19
- 8.4 FPC Layers 20

Appendix A. Revision History 21

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1.0 INTRODUCTION

This document provides basic ground rules to be observed when executing a printed circuit board layout for use with Microchip maXTouch touch controllers. Many of these rules are basic common sense guidelines which will have been used in previous PCB designs.

Adhering to these guidelines will ensure that the final product stands the best chance of passing any EMC or ESD tests that the equipment will be subject too, both in terms of defending against external aggressor signals interfering with the touch system and minimizing emissions from the touch controller.

It should be noted that no amount of rules or guidelines can guarantee product conformance with environmental requirements, as each design is unique, and will present its own set of problems.

The information presented in this document is not specific to any particular Microchip touch controller product, therefore parts of this document may be ignored if they are not appropriate for the current design.

This document represents best practice for new designs, and is subject to change as and when new products are introduced.

Many of the requirements are common to touch sensor design, and this document should be read in conjunction with the following document:

- QTAN0080, *maXTouch Sensor Design Guide*

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2.0 INITIAL PREPARATION

Initial preparation for a new printed circuit board layout is **very important**, and should take into account such factors as component placement/orientation and supply routing. Components should be orientated such that signal and power tracking is as efficient and short as possible. This applies particularly to the routing of the X and Y lines between the controller and the touch screen – especially if the touch controller is to be used in the self capacitance mode. After this, the routing of the power and ground traces should be considered. Thought should be given to the positioning of supply rail decoupling capacitors and supply rail tracking. These two are vital to the correct operation of the circuit, and also to ensure that EMC requirements are met in relation to emissions and immunity. Careful placing of supplies and supply decoupling capacitors can help reduce the number of decoupling components required, while still ensuring satisfactory touch controller performance.

3.0 TRACE ROUTING

When routing signal, power, X and Y traces, there are some important guidelines that should be followed, as described in the following sections.

3.1 Signal Tracking

Care should be taken to ensure that signal tracks, especially those with fast edges, are kept as short as possible. Also of vital importance is to ensure that such signals (which include clocks, SPI or I2C buses and similar) have a full and unbroken GROUND signal return path which runs the full length of the signal track. Any discontinuities in the ground return path will result in signal reflections and potential noise radiation from that track. Note that this specifically does NOT apply to X and Y tracking between the controller and touch screen. These tracks are dealt with later in this document.

Inter layer vias should be avoided for all high speed signals, as these impose additional inductance and stray capacitance on the signal. A via will also usually violate the integrity of the all important ground return path. As in all designs, some compromises must be made, and it may not be possible to adhere to this rule at all times.

It should also be ensured that high speed signal tracks do not make sharp directional changes. Direction changes of more than 45 degrees should be avoided. Ninety degree direction changes should, for example, be replaced with two 45 degree bends. This will avoid abrupt impedance changes which are the cause of signal reflections along the track, and radiated noise from an electronic circuit. Remember that each signal line has the ability to both radiate RF energy and be susceptible to any local RF fields. Keep all susceptible tracks short, and view all signal tracks as if they were small antennas.

3.2 Track Width Rules

The width of individual tracks should be chosen to ensure that current handling and other characteristics are observed for each signal. Power tracking should be kept as wide and heavy as possible to ensure minimum inductance and voltage droops.

3.3 Board Layers

A four layer design, if properly executed, will ALWAYS out perform a two layer board in terms of EMC and ESD immunity. In the four layer case, it is assumed that the extra two layers are used to provide a solid ground and power plane on the inside of the board, with the signal tracking on the outer layers. Whether a two or four layer board design is undertaken almost always involves weighing the benefits of the four layers against cost. A four layer board will improve the integrity of signals and reduce supply noise and ripple, and will also ensure that noisy signals are kept within the confines of the outside (grounded) layers, avoiding emissions and susceptibility. A two layer board layout becomes more critical and difficult to implement because of the inevitable compromises that must be made when tracking in power and signals.

3.4 Y Lines

The Y lines are the most critical in terms of layout. They are not themselves touch sensitive when operating in the MUTUAL CAPACITANCE mode. In the SELF CAP mode, however, they become an integral part of the touch sensor, and therefore need to be carefully tracked. These tracks should be kept as short as possible, and should be kept away from ground planes or other signal tracking. Particular care should be taken if designing a layout for both mutual and self capacitance modes. See Section 3.6 “Guard Track (Self Capacitance Measurements)” for more information.

Observe the following points:

- Minimize the trace lengths between the IC and the sensor.
- Avoid running Y lines over or between ground or power planes wherever possible to help minimize stray capacitance.
- Try to keep parasitic routing capacitance on each Y line to less than 50 pF (to ground or other low impedance circuits) between the device and the sensor hot-bond.
- The parasitic series resistance of each Y line should be kept to less than 100Ω from the device to the sensor hot-bond.
- Always route Y traces using minimum track and gap geometries, and route them as a group all the way from the device to the sensor.
- Do not route the Y lines in parallel to (and above) the X lines, such as on opposite sides of a flex.

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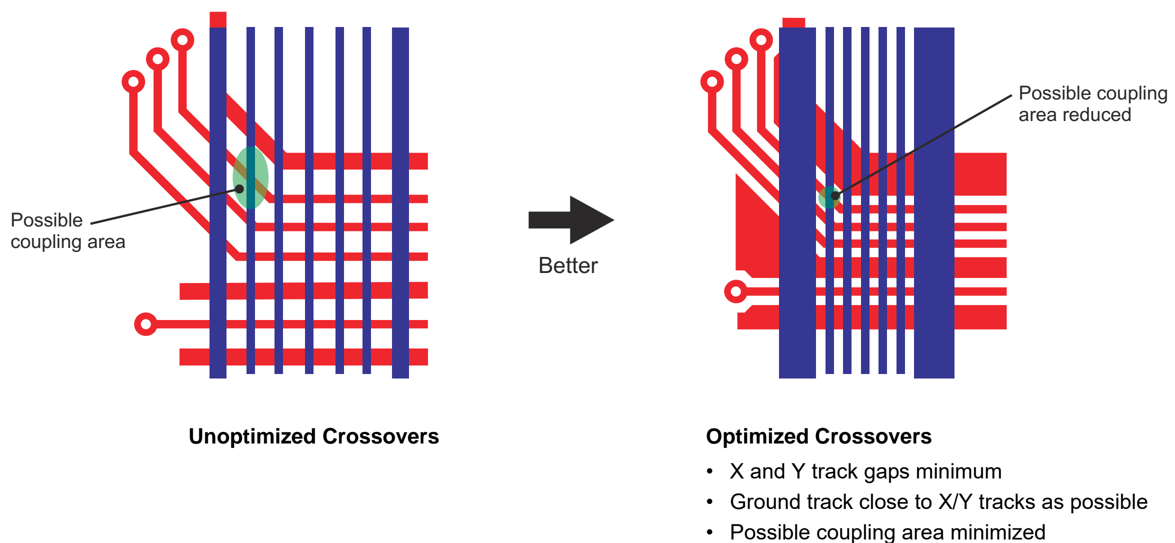
- Separate the Y lines from the X lines using at least a double width or double gap ground trace between the groups of signals, or driven shield trace if using self cap. This converts coupling (mutual) capacitance into stray capacitance, which is more tolerable.
- If using self capacitance mode, place a driven shield (guard) track between the Y lines and any Ground as well. See Section 3.6 “Guard Track (Self Capacitance Measurements)” for more information on a driven shield track for self capacitance layouts.
- If the Y lines must cross the X lines on opposite layers, cross them at 90° and, ideally, far away from any touchable regions. Cross them on layers that are as far apart as possible, ideally separated by a Ground layer.
- Keep foreign signals (for example, communications signals, data buses or strobes) well away from the Y lines.

FIGURE 1: OPTIMIZING CROSSOVERS



Unoptimized Crossovers

Optimized Crossovers

- X and Y track gaps minimum
- Ground track close to X/Y tracks as possible
- Possible coupling area minimized

3.5 X Lines

The X lines are as important as the Y lines if the self capacitance mode is to be used. They are not themselves touch sensitive when operating in the mutual capacitance mode. However, in the self capacitance mode, they become an integral part of the touch sensor, and therefore need to be carefully tracked. These tracks should be kept as short as possible, and should be kept away from ground planes or other signal tracking. Care should be taken if designing a layout for both mutual and self capacitance modes. See Section 3.6 “Guard Track (Self Capacitance Measurements)” for more information on a driven shield (guard) track for self capacitance layouts.

Observe the following points for both X and Y lines:

- Minimize the total routed length from the device to the sensor’s hot-bond.
- Avoid excessive capacitive loading on the X lines to ground. Refer to the datasheet for your device for loading characteristics.
- In general, do not place any component in series or parallel with the X lines. However, if they are required for EMI control, series damping resistors of up to 1 kΩ may be used.
- All X lines should be routed as a group, as should the Y lines.
- See the notes on Y lines in Section 3.1 “Signal Tracking” for X to Y separation rules.
- The series resistance of each X line (not including extended X line resistance) should be kept to less than 100Ω from the device to the sensor hot-bond.

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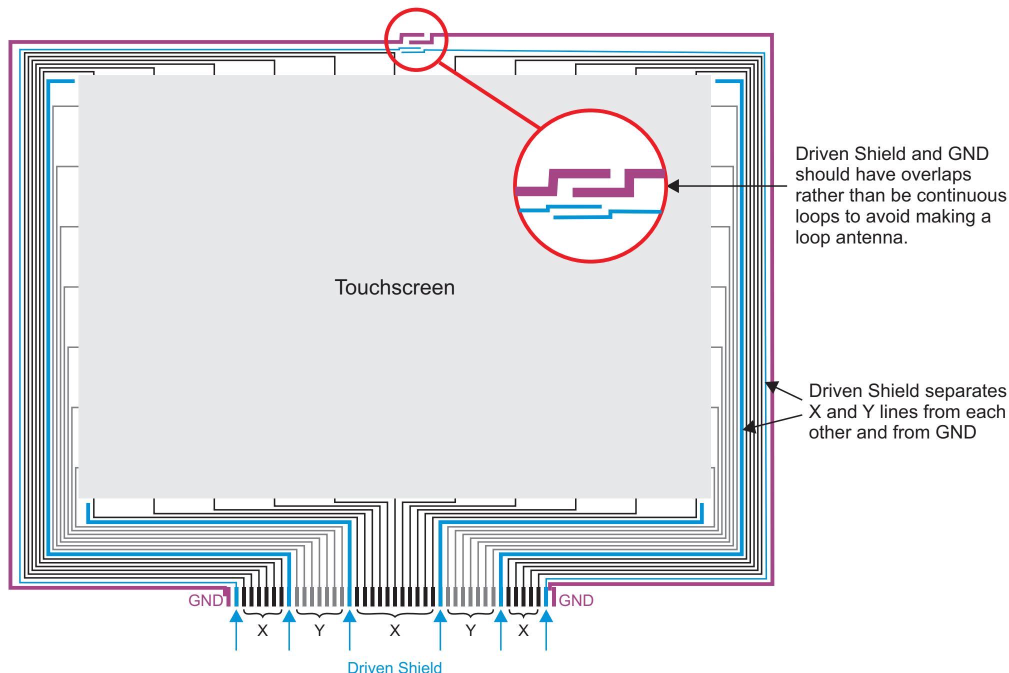
3.6 Guard Track (Self Capacitance Measurements)

When the maXTouch device operates in self capacitance mode, the X and Y lines are equally critical, as both become touch sensitive in this mode. If self capacitance operation is supported, therefore, a guard track in the form of a driven shield (typically the DS0 pin) must be placed in between X and Y lines to keep them separated (see Figure 2). The guard track also needs to separate the X and Y lines from Ground.

Note that the Ground track should separate the X and Y lines from other signals or power supplies on the board. If this is not possible, due to design restrictions, the driven shield track will also have to shield the X and Y lines from these other traces.

The driven shield track traces should be restricted to narrow traces on the PCB. That is, no large areas of copper should be used to avoid "slowing" the driven shield signal. In order to avoid making a loop antenna, the driven shield traces should not form a continuous loop, but should instead be implemented using overlaps. See Figure 2 for details.

FIGURE 2: EXAMPLE DRIVEN SHIELD ROUTING



NOTE: Sample touchscreen for illustrative purposes only. The number of X/Y lines available on any given device might differ from that shown here. Similarly, the routing of the X/Y lines shown should not be taken as indicative of any preferred layout and the user's layout may vary.

3.7 Shielding and Ground

Where shielding layers are placed over an FPC, these should be connected to Ground, not the driven shield pin (DS0). Although this will create extra parasitic capacitance to Ground for the X and Y lines, the shielding layers cannot be connected to DS0 because the large capacitive load will exceed the drive capability of the DS0 pin and stop it fulfilling its purpose of isolating the "real" X and Y traces from ground loads. Ideally such shield layers should be hatched, not a full flood, but externally laminated ESD shielding does not normally cause an issue.

3.8 ESD Ground Routing

To protect the maXTouch device from ESD discharges, the outermost track on the sensor should be an ESD ground (see Figure 3). Like the driven shield, this should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

To avoid electromagnetic induction of currents into the driven shield trace, a minimum separation of 0.3 mm should be maintained between the ESD Ground trace and the Driven Shield.

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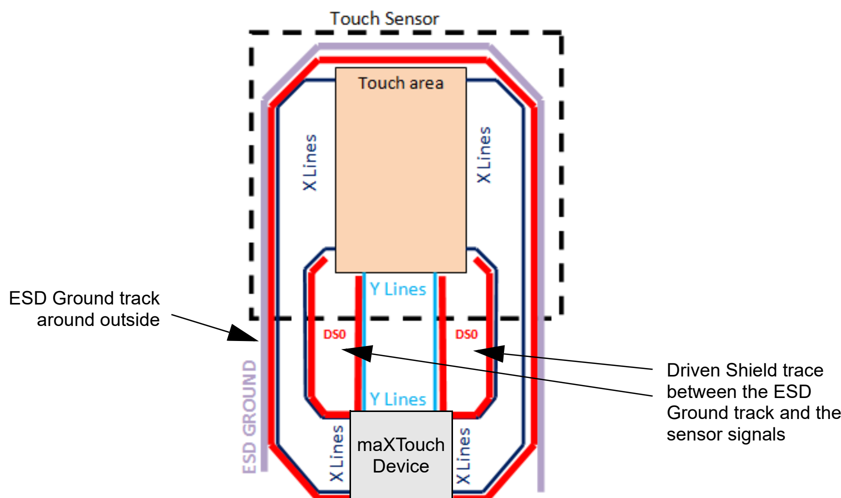
The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main Ground connection to the PCB.

FIGURE 3: ESD GROUND



3.9 Power Traces

Power to the maXTouch device is provided via three or four sets of pins: Vdd (digital supply), AVdd (analog supply) and XVdd (external high voltage supply). Additionally the IO interface to the host can be referenced to a separate VddIO voltage instead of being common with Vdd. Keep these traces as thick as possible to keep inductance low.

With good board layout, (including the use of power and ground planes), a single capacitor can suffice for decoupling each supply, however, as many capacitors as desired may be added to compensate for less than ideal power tracking (for example, on a two layer board), or a noisy common supply.

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

A parallel combination of capacitors is recommended to give high and low frequency filtering. This is beneficial if the voltage regulators are likely to be some distance from the device (for example, if an active tail design is used). Note that this requires that the voltage regulator supplies are clean and noise free. It also assumes that the track length between the capacitors and the on-board power supplies is less than 50 mm.

3.10 Vdd

This is the digital supply to the device. It is independent of the analog supply. Refer to the datasheet for your maXTouch device for allowable ranges.

Vdd is not directly used as part of the capacitive measurement process and so it is relatively tolerant of noise.

While the average power used by Vdd is low, the instantaneous peak current on Vdd means that good quality supply bypass capacitors must be used very close to the device body (within 5 mm). Vdd must be regulated by the host system and is commonly supplied from the same power rail that serves the rest of the host’s digital domain.

While it is possible to run Vdd and AVdd from the same supply, this may have noise implications if good layout and high quality capacitors are not used.

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3.11 AVdd

This is the analog supply to the device. It is independent of the digital supply. AVdd is critical to the performance of the device and is used directly by the measurement front end.

The instantaneous peak current demand on AVdd means that good quality supply bypass capacitors must be used very close to the device body (within 5 mm). It also means that series inductors cannot be used to isolate the digital and analog supplies if sourced from a common regulator. Instead, create a star point at the regulator output and run separate, low-impedance traces for Vdd and Avdd (see Section 3.15 “Low Drop-out Voltage Regulators”). Refer to the datasheet for your maXTouch device for recommended values and types.

3.12 XVdd

XVdd is the X line drive power supply. In normal mode, XVdd is connected to the AVdd analogue power supply. In many maXTouch devices, XVdd can also be connected to an external high voltage analogue supply in high voltage mode. This may be an on-board booster supply or an external high-voltage rail. Some maXTouch devices generate their own XVdd from the Vdd or Avdd rail. See Section 5.0 “External High Voltage Circuit Layout” and refer also to the details in the datasheet for your device.

All XVdd related components are required to be placed very close to the XVdd pins of the maxTouch device. Once again, instantaneous peak current on this rail is high, so tracking must be thick, suitably decoupled and as short as possible. Suitable derating of capacitor operating voltages should be observed if high voltage XVdd is used.

3.13 VddCORE

Most Microchip touch controller family members operate with a separate core voltage. This voltage is provided by an internal LDO (derived from Vdd), and decoupling capacitors for this supply should be placed close to the pin. Refer to the datasheet for your maXTouch device for decoupling requirements.

3.14 Ground

There are multiple Ground pins on the device. Connect them all to a single low impedance ground trace or flood. DO NOT rely on internal connections between ground pins. Some devices also have a ground pad underneath the device: if present, this must also be grounded. Refer to the datasheet for your device for details.

Ground trace routing should be carefully considered. Do not share the touch controller ground return path with other chips in the design (apart from LDOs that solely power the maXTouch device), as this may induce noise in the capacitive measurements and thereby reduce the signal-to-noise ratio of the system. A better solution is to try to run a single wide trace back to a common star-point at the supply origin. A flood is preferable to a ground trace as it will reduce the current density flowing under the device; best of all is a split flood, to ensure that other ground currents does not affect the device’s ground reference at all.

Local regulators solely supplying the maXTouch device should be located as close as possible to the maXTouch device and the loop size of the power/ground path should be minimized.

These approaches (both good and bad) are summarized in Figure 4.

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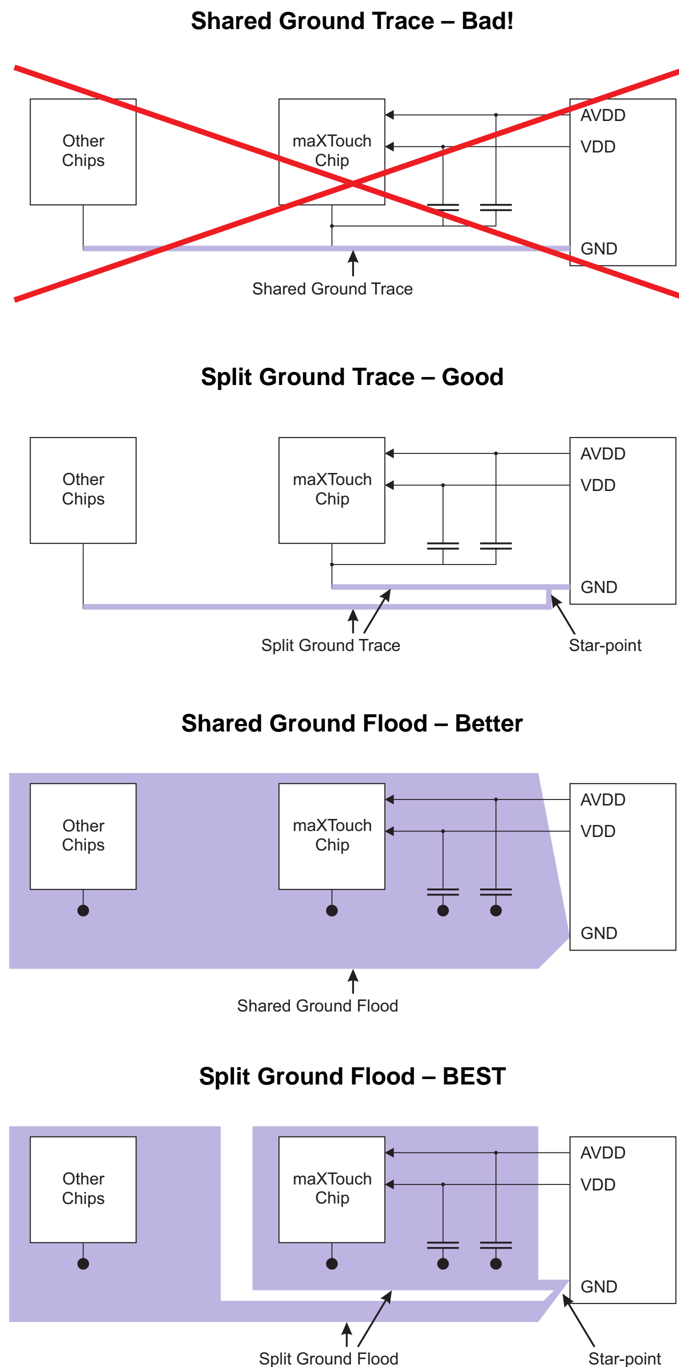
FIGURE 4: GROUND TRACE ROUTING PREFERENCES



The topology of the ground (and power) tracking in any PCB layout should be determined during the initial preparation phase of the design. It is too important to leave this until later stages of the design. New designs should always strive to achieve the best solution, as defined in the diagrams above for ground tracking. This applies to both two and four layer designs.

It is particularly important to route ESD ground return paths away from the maXTouch device. An ESD discharge can result in high peak currents and sharp rise-times, which can induce high voltages onto other traces running close by. Do not allow such currents to flow underneath the maXTouch device and separate any ESD return trace by at least 0.3 mm from a driven shield or similar line. It is recommended that the ESD trace runs around the perimeter and connects to a star point near the Ground input connector

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3.15 Low Drop-out Voltage Regulators

3.15.1 SINGLE LOW DROP-OUT VOLTAGE REGULATOR SUPPLY

When designing a PCB for an application using a single Low Drop-out Voltage regulator (LDO), the traces for Vdd and AVdd should be split as close as possible to the regulator, ideally adjacent to the LDO footprint. This separates the AVdd current flows in AVdd from those in Vdd, thus minimizing the noise introduced into AVdd from Vdd. The two power supply traces should be routed over a ground plane as much as possible. They should not be routed close together as this will introduce unwanted coupling between them.

There are three options for routing with a single LDO:

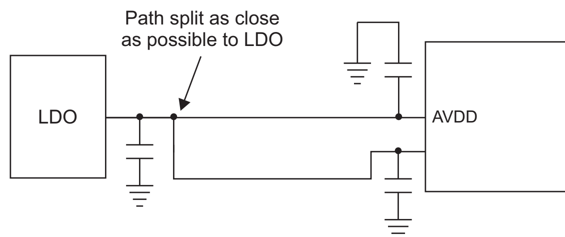
- **LDO near touch controller** – split power traces near LDO

  The best option is to place the LDO on the same PCB as the touch controller, and close to it. In this case, the traces for AVdd and Vdd should split as close as possible to the footprint of the LDO.

  For information on the reservoir capacitors next to the touch controller refer to the data sheet for your device.

  It is possible that an additional capacitor next to the LDO will be required for reasons of LDO stability. Refer to the chosen LDO manufacturer's data sheet for guidance.

FIGURE 5: PREFERRED SINGLE LDO OPTION



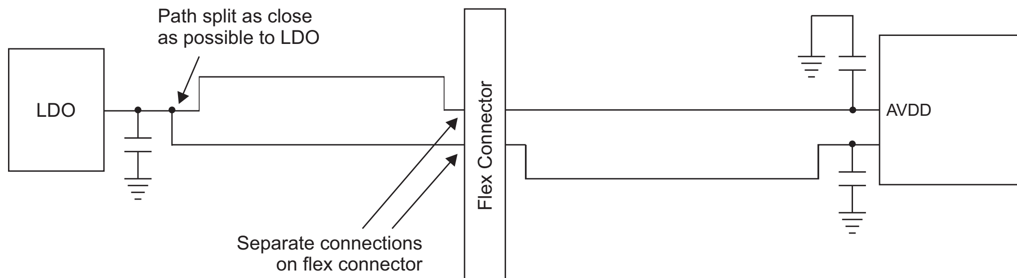
- **LDO remote from touch controller** – power traces split near LDO

  If the LDO must be remote from the touch controller, the best option is still to split the traces for AVdd and Vdd next to the LDO and route them separately from there. Figure 6 shows how this would be implemented in a case where the LDO were on the main PCB and the touch controller on a flex. In this case, two separate connections are used on the flex connector.

  For information on the reservoir capacitors next to the touch controller refer to the data sheet for your device.

  An additional capacitor next to the LDO may be required for reasons of LDO stability (including when a flex is not connected). Refer to the chosen LDO manufacturer's data sheet for guidance.

FIGURE 6: REMOTE LDO – POWER TRACES SPLIT NEAR LDO



- **LDO remote from touch controller** – power traces split away from LDO

  If it is not possible to split the AVdd and Vdd traces next to the LDO, then the split should be made as close as possible to the connector for the PCB or flex carrying the maXTouch device. This minimizes the coupling of interference into the touch controller AVdd. The trace from the LDO to the split should be especially wide to minimize impedances along it. Figure 7 shows the situation where the LDO is on the main PCB, the touch controller on a flex, and only one connection is available through the flex connector. In this case the supply traces should split on the flex, next to the flex connector.

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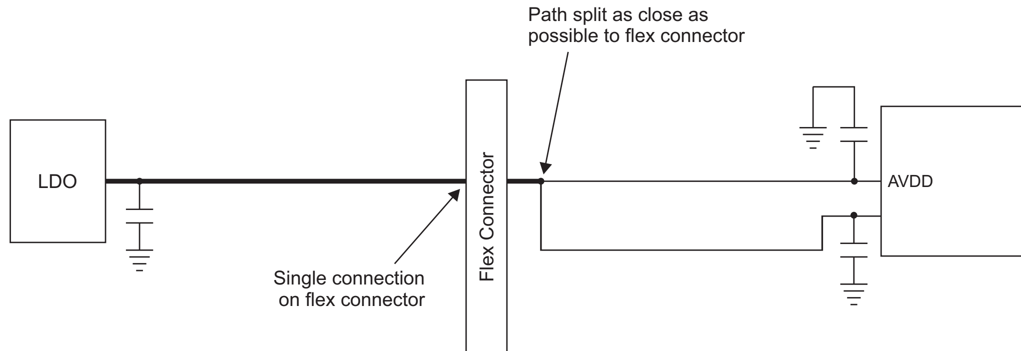
For information on the reservoir capacitors next to the touch controller refer to the data sheet for your device.

An additional capacitor next to the LDO may be required for reasons of LDO stability (including when a flex is not connected). Refer to the chosen LDO manufacturer’s data sheet for guidance.

FIGURE 7: REMOTE LDO – POWER TRACES SPLIT NEAR FLEX CONNECTOR



3.15.2 MULTIPLE LDO REGULATOR SUPPLY

The AVdd supply stability is beneficial for the device because this supply powers the sensitive circuits of the analog front end. If noise problems persist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This minimizes the amount of noise injected into the sensitive, low signal level parts of the design.

As Vdd and AVdd do not have to be the same voltage level, another good option is to have one main LDO or power supply for Vdd, and then derive a local AVdd supply from that using a Microchip Ripple Blocker™ device. As above, it is best to place this as close as design will allow to the main supply chip.

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4.0 COMMUNICATION TRACES

4.1 SPI Traces

The length of the SPI traces should be kept to a minimum. Particular attention should be given to the SCK trace which can be noisy. Ideally, route the SPI bus traces together as a group.

4.2 I²C Traces

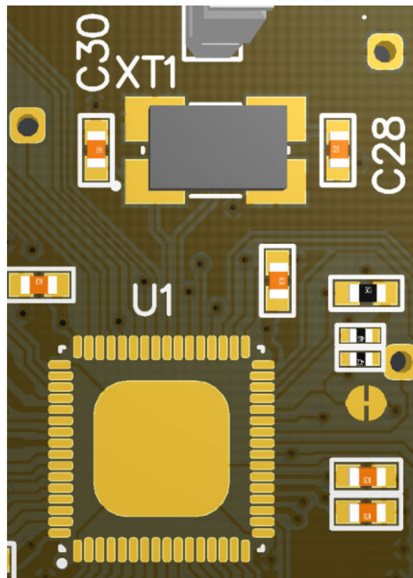
Always route SDA, SCL, and $\overline{\text{CHG}}$ lines well away from the Y lines to avoid any potential coupling and hence noise contamination.

There are no internal pull-up resistors in the maXTouch device so external pull-up resistors are required for SDA and SCL. These resistors must be connected to the VddIO supply, or to Vdd if a separate VddIO supply is not present. The $\overline{\text{CHG}}$ line is also open drain, and so this will also require a pull-up resistor to VddIO (or Vdd if there is no separate VddIO supply) somewhere in the circuit. It is worth checking with the design authority whether these resistors have been catered for (such as in the host-side circuitry), or whether they are needed on the current design.

4.3 Crystal Selection

If a crystal is required by the maXTouch device, this and its accompanying load capacitors must be kept as close as possible to the controller pins, making sure to keep all other signals as far away as possible. Oscillator circuits are high impedance, and are therefore sensitive to noisy tracks running adjacent to or underneath them. A ground plane under the crystal and its tracking to the controller is recommended (see Figure 8).

FIGURE 8: CRYSTAL LAYOUT



4.4 Other Traces

$\overline{\text{RESET}}$ – routing is non-critical, and is generally tied to a high logic level. If left open circuit, however, care should be taken that there are no adjacent noisy signals, which could cause false resetting. It has been found that in some cases, a 10n or similar value capacitor from the reset line directly to ground can assist in improving the ESD immunity of the board. In such cases, this cap (and its associated pull-up resistor) should be tracked very close to the reset pin on the device.

ADDSEL, MODE SELECT and similar signals – routing is non-critical. It is sampled only at start-up or reset to select the required I²C client address.

GPIO – routing for GPIO lines should be kept as short as possible, and like all other signal tracking, should avoid vias, and any breaks in the signal return path (ground).

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4.5 ESD Handling

The best way of handling ESD for a touch sensor is to prevent it getting in at all: the small geometries and materials of a touch sensor mean it can be vulnerable to physical damage from an ESD strike. The whole system (sensor, FPC and host board) should be designed with an eye towards ESD compliance. Following the guidance for PCB and FPC design elsewhere in this document should be of help here.

Typically, the design rules (track size and spacing, minimum cut widths, minimum geometry size, and so on) for a given project are defined by the manufacturer based on a balance of their process capabilities and cost structure for the project. The precise approach to handling ESD will therefore depend on the manufacturer's specifications. Nevertheless, the following provides some general guidance for handling ESD:

- The distance between the ESD Ground trace and the sensor traces should be maximized where possible. A distance of 0.3 mm is considered reasonable, but some manufacturers consider 0.5 mm to be the preferred minimum. The actual distance chosen depends greatly on the stack and the materials used: some OCAs, for example, are more conductive than others.
- The width of the ESD Ground trace should be maximized where possible, to reduce the resistance. Again, there may be manufacturer's guidance to comply with here.
- For ground and power tracks, ensure that multiple vias are placed between the tracking on different layers. Avoid using single via connection points between these tracks. This is particularly important where a dedicated ground plane is used, as the multiple connections will ensure a solid connection to Ground.
- ESD currents should be routed away from the maXTouch device. Where Ground is used instead of Driven Shield for isolation between X and Y lines, ensure that the ground traces or flood will not form part of the ESD strike ground return path.
- All metal near the sensor should be solidly grounded. Areas of floating metal near the sensor should be avoided, as these will have a direct impact on the ESD and touch performance. It is possible to have small areas of conductive metal (for example, printed silver graphics), but the spacing to the sensor is important and it is not an ideal scenario.
- The use of series resistors on the sense lines can be considered for ESD protection and these are preferred to the use of inductors. A value of 1K0 is recommended, with a maximum of 2K7. Resistors on the X lines improve radiated emissions (slower edge rate) but tend to increase the charge time (which means a longer ADC acquisition window and more opportunity for noise injection). Resistors on the Y lines help somewhat with emissions and also assist with ESD protection.
- The use of ESD protection devices (TVS diodes) can be considered as an alternative. As a rule, these should be applied to any part of the design which may be susceptible to high voltage and could be affected by a close ESD discharge, or which would have close or direct contact with an external entity, such as an equipment operator. The requirement for such protection devices will very much depend upon the overall system design and layout of an individual product, and whether or not the controller is close enough to potential discharge sources to present a problem.
- However, due to their nature, most ESD protection devices will introduce a fairly large capacitance burden to the circuit they are protecting. For this reason, these protection devices typically cannot be used on the X or Y lines of a touch controller, or any other high speed signal lines. In addition, the component cost and PCB real estate requirements would probably preclude this.
- Good candidates for the addition of an ESD protection device include power supplies, where these are brought onto the PCB via long cables, and any exposed parts of the circuit which are likely to be directly contacted by the equipment operator or user.
- For further advice, and design reviews, please contact your Microchip representative.

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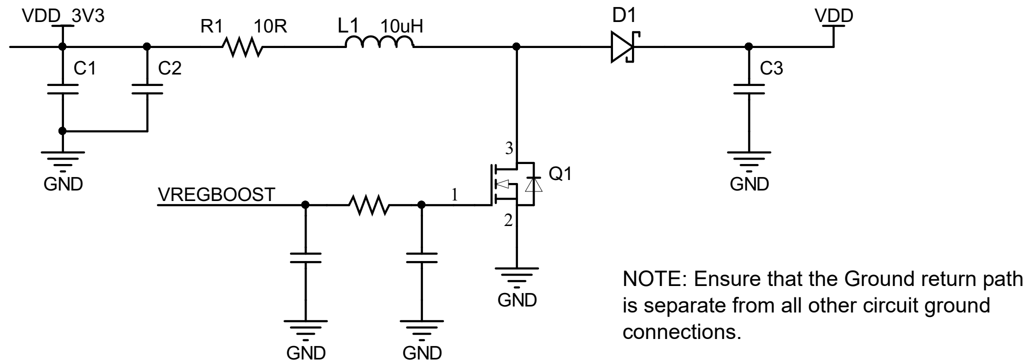
5.0 EXTERNAL HIGH VOLTAGE CIRCUIT LAYOUT

If an external high voltage supply is used special attention must be given to the component placement.

FIGURE 9: EXAMPLE OF A BOOST CONVERTER CIRCUIT



In the example shown in Figure 9, the components for the boost converter circuit must be placed very close to each other especially the inductor, diode (D1), capacitors (C1, C2, C3) and the switching FET. The inductor chosen should be a screened type, with a high self-resonant frequency. Refer to the boost converter chip manufacturer data sheet for more details. For typical component values, refer to the datasheet for your device.

As discussed in Section 3.14 “Ground”, the ground for the boost converter is best split from the common ground of the touch controller and connected only through a star-point connection. This star connection should be as close to the power entry point on the PCB as possible.

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6.0 BGA ESCAPE ROUTING

FIGURE 10: EXAMPLE 64-BALL BGA ESCAPE ROUTING PATTERN ON 2-LAYER PCB

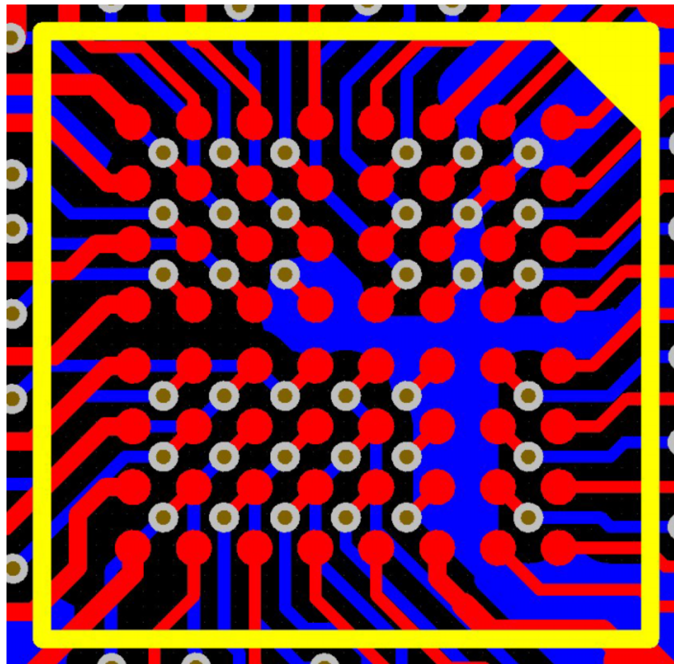
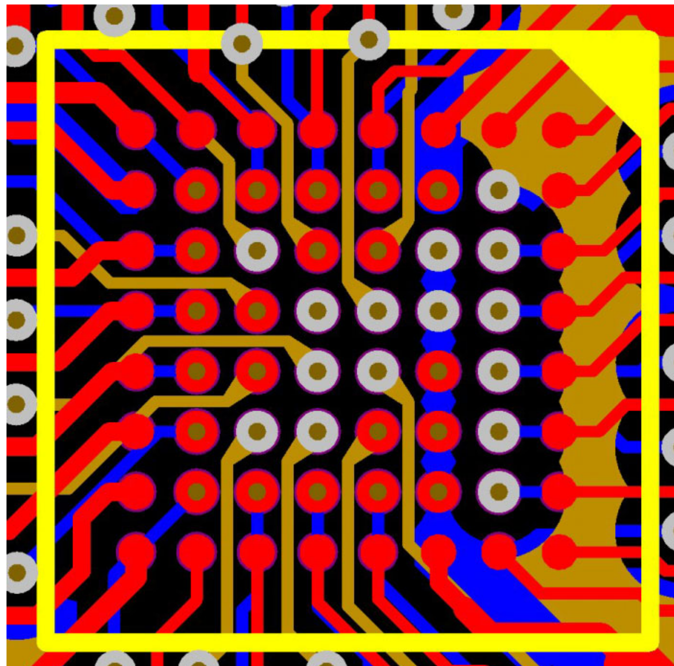


FIGURE 11: EXAMPLE 64-BALL BGA ESCAPE ROUTING PATTERN ON 4-LAYER PCB WITH VIAS IN PAD



7.0 DESIGN FOR MANUFACTURING

7.1 Layout Traces

Typical track width is 0.15 mm with 0.15 mm clearance gap. However, width and copper clearance capabilities may vary between different manufacturers.

To escape the BGA package tracks will need to neck down to 0.1 or even 0.080mm to enable routings in between vias. Copper clearance will also need to reduce to 0.1 mm and sometimes lower depending on the via annular pad size. Typical smallest clearance between copper is 0.080mm with a good manufacturer.

7.2 Vias

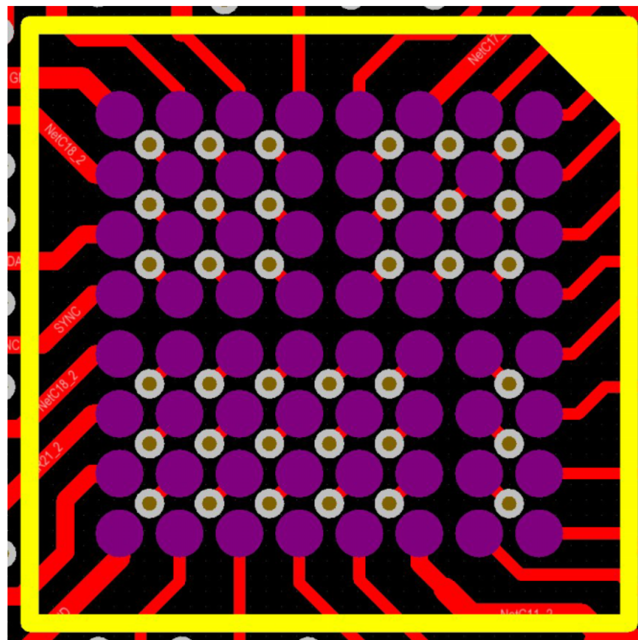
Vias are used to escape tracks from the inner balls of the BGA package. In general, the size of a via is determine by its aspect ratio – the depth of the via against the drill hole size before plating.

Laser drilling must be used for BGA routing escape, as less than 0.15 mm drill size is required. Typical laser drill size is 0.1 mm (100 micron). The aspect ratio is an important factor. Laser drill is more commonly used in FPCB where the stackup or materials used are thinner than rigid PCB. When designing multilayer FPCB (3 layers or more), always get the advice from the manufacturer if whether 0.1 mm drill is still possible. Manufacturing limitations may vary from one manufacturer to another.

7.3 Solder Mask

Solder masks provide a permanent protective coating for the copper traces of a PCB and prevent solder from bridging between conductors, thereby preventing short circuits. Figure 12 shows a solder mask in the negative. For BGA package, ensure vias and tracks in between the balls are covered with a solder mask.

FIGURE 12: VIAS AND TRACK IN BETWEEN BGA BALLS MUST BE COVERED WITH SOLDER MASK



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7.4 Layer Stack-up

Most of the maXTouch devices with a small node count can be designed on a minimum two-layer PCB. However, due to different design constraints which may be required in the design request, the number of layers may increase up to four layers.

Figure 13 and Figure 14 show two different proposals for layer stack-ups for a typical maXTouch design.

FIGURE 13: STACK-UP FOR 2 LAYER PCB

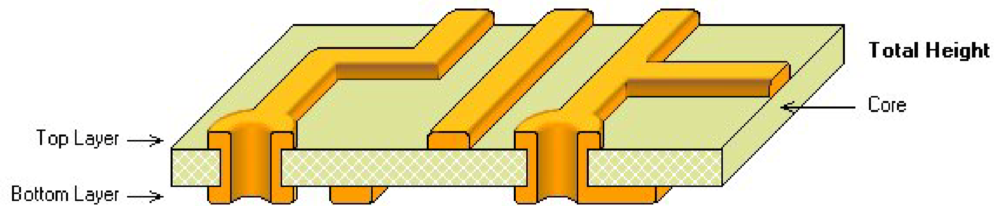
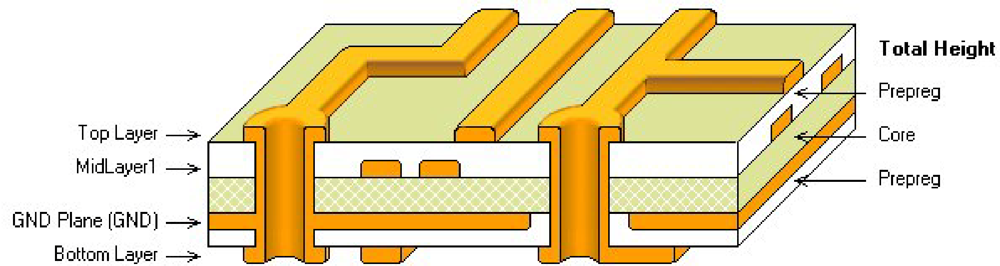


FIGURE 14: STACK-UP FOR 4 LAYER PCB



8.0 FLEXIBLE PRINTED CIRCUIT

All the rules of a PCB layout as stated above will apply to a flexible printed circuit (FPC). However, due to its flexibility, designing an FPC will require additional rules for a successful layout. There are basically two types of FPC, which are:

- **Passive** – Single-sided or double-sided flex with no components. Passive FPC is typically used for making interconnections between PCBs by means of an FFC connector.
- **Active** – FPC with electronic circuits printed on the flex. For an active FPC, a stiffener is attached to the component area to support the weight of the electronic components.

8.1 FPC Layout

The layout rule on an FPC will generally be similar to a standard PCB. However, care should be taken especially in the area where the FPC will be folded, also called the bending area.

A few design rules should be taken into consideration when routing in the bending area.

- **Tracks** – All tracks going through the bending area of an FPC must be routed in straight lines. Avoid routing the tracks in 45 or 90 degree angles. If a straight track is not possible, the traces should be routed using a curved angle.
- **Via** – No vias should be placed in the bending area.
- **Copper Pour** – Having a copper pour filled in the bending area will directly affect the flexibility of an FPC. If it is really necessary to have copper pour within the bend region (for example, for technical reasons such as shielding the X and Y from coupling), try using a 40% hatched pour instead of solid pour. Note that a hatched copper pour will have the same electrical shielding properties as a solid layer, but will not load adjacent signals as much.
- **Number of Layers** – Only use a maximum of two layers for trace routing and layout in the bending area. Avoid using more than 2 layers because this will affect the flexibility of the FPC. For example, if the FPC is using four layers, choose Mid Layer 1 and Mid Layer 2 for trace routing in the bend region. The Top and Bottom layers should be free from any tracks and copper.

FIGURE 15: EXAMPLE OF LAYOUT IN BENDING AREA ON A 4 LAYER FPC

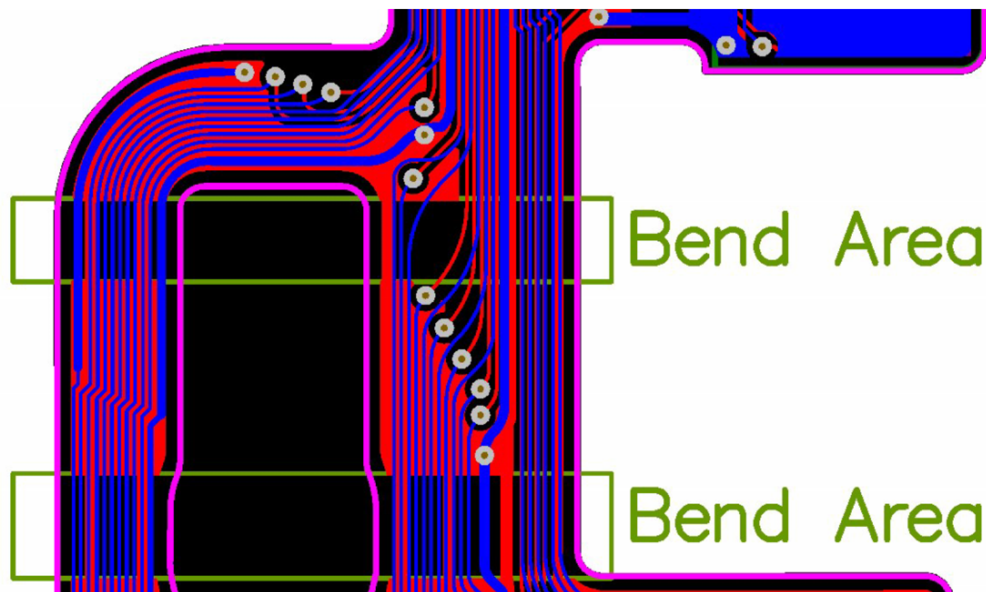


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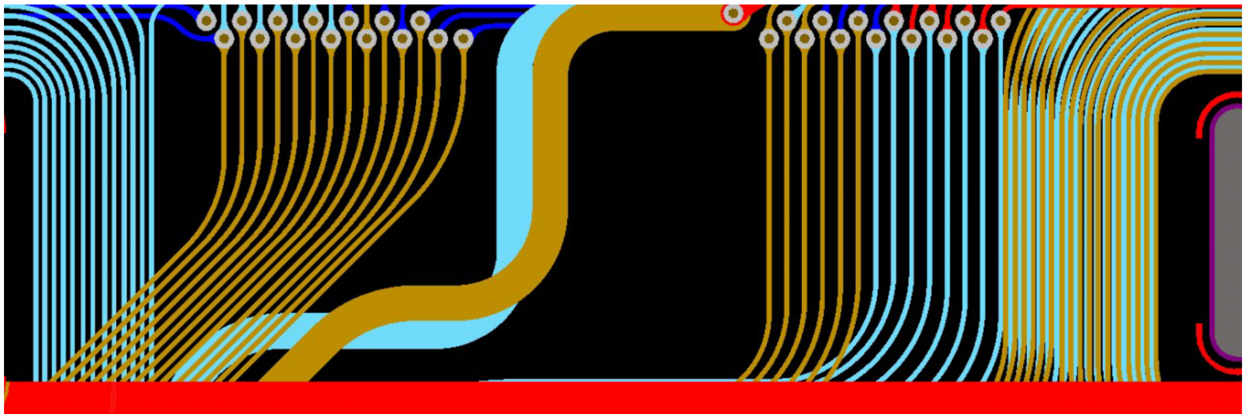
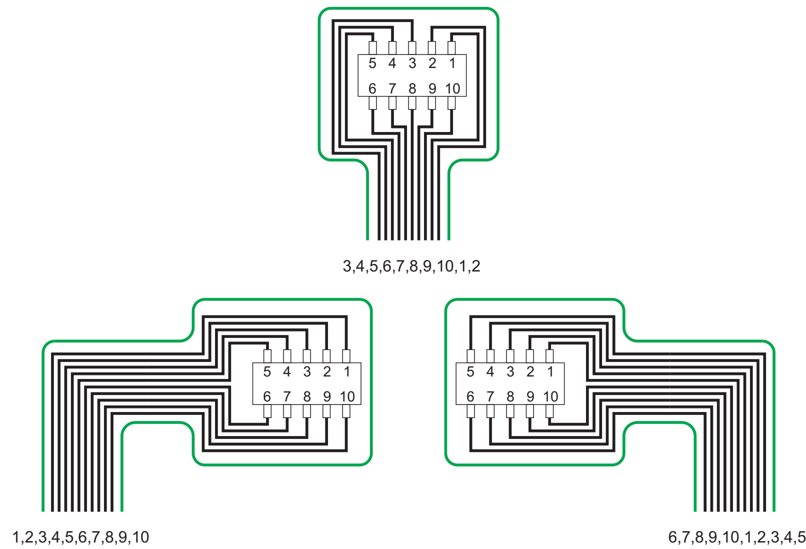
FIGURE 16: EXAMPLE OF LAYOUT IN BENDING AREA ON A 2 LAYER FPC



8.2 FPC Orientation

The shape and direction of the connector stub influences the tracking pinout. Figure 17 shows three scenarios that illustrate different tracking layouts using the same connector pinouts.

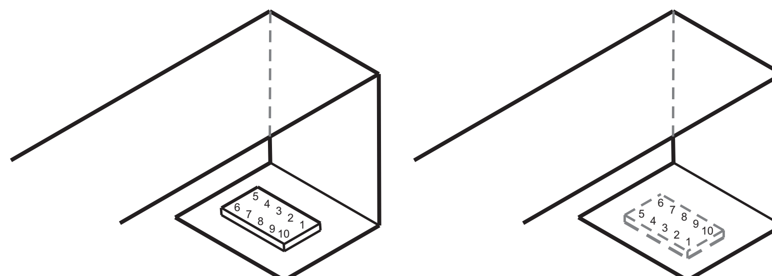
FIGURE 17: SCENARIOS FOR TRACKING PINOUTS



8.3 FPC Folding Path

Depending on which side the connector is attached to both the FPC and the soldered side of the connector on the main board, the pinout may be mirrored or rotated as the result of one small change (see Figure 18). This can, of course, be "corrected" using vias if there is enough space.

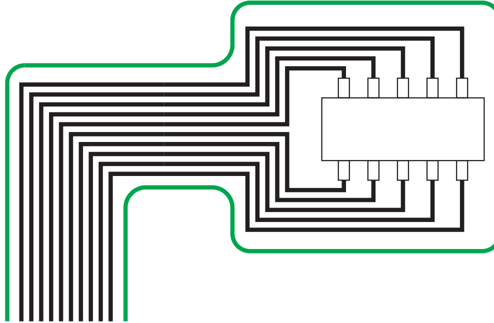
FIGURE 18: FIGURE 20 FPC FOLDING PATH



8.4 FPC Layers

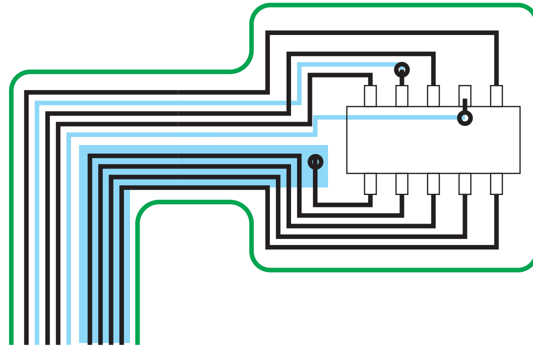
Using a one-layer FPC (see Figure 19) results in a limitation on the possible pinouts. In this case, shielding is also not possible

FIGURE 19: ONE-LAYER FPC



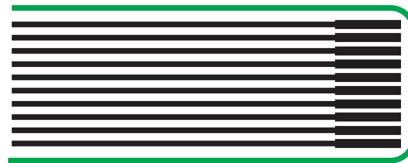
A two-layer FPC (see Figure 20) allows for much more flexibility in the pinout, tracking and shielding options, but remember to keep X-Y coupling to a minimum.

FIGURE 20: TWO-LAYER FPC



A FPC ZIF style connector makes the choice of pinouts more difficult as there are fewer convenient spaces for vias (see Figure 21).

FIGURE 21: TWO LAYER FPC – ZIF STYLE CONNECTOR



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APPENDIX A: REVISION HISTORY

Revision CX (November 2016) – Atmel edition

Final Atmel revision

Revision A (August 2021) – Microchip edition

Reformatted and updated – Microchip edition

This revision incorporates the following updates:

- Updated to Microchip application note format:
  - *Table of Contents* added
  - *Associated Documents r*emoved
  - *Revision History* moved to this appendix
  - Back cover updated
- Changes to content:
  - PTC key information removed
  - Information on generic/auxiliary keys added
  - Section 5.0 “External High Voltage Circuit Layout” updated
  - Other minor changes to advice
- New documentation number assigned

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ISBN: 978-1-5224-8773-9

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