Understanding the Impact of Single Event Effects in Networking Applications

Introduction (Ask a Question)

Reliability of communication is essential in networking applications. The goal of five nines (99.999%) in network availability translates to less than six minutes of downtime in a year for the entire network. Among the many impacts on system reliability are the effects of ionizing radiation on electronic circuits. This radiation can cause memory elements in electronic circuits to change state. When this happens in the configuration memory of SRAM-based FPGAs, it can cause a change in the functionality of the circuit, greatly impacting system reliability. Designers of networking applications must understand the effect of this radiation and how to reduce the risk to the network.

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1. Sources and Effects of Ionizing Radiation (Ask a Question)

The following sections discuss the sources and the effects of ionizing radiations.

1.1 Galactic Cosmic Rays (Ask a Question)

Galactic Cosmic Rays (GCR), comprised of high-energy particles, overwhelmingly protons, impact the Earth's atmosphere constantly. These particles, originating in space, have sufficient energy to liberate nuclei when they collide with molecules in the Earth's atmosphere. The result of this collision is referred to as an air shower, where a wide range (and high number) of particles are generated. The primary spallation products of concern are neutrons and protons (in addition to remnant cosmic rays).

The flux of cosmic rays impacting the Earth's atmosphere is modulated by both the solar wind and the Earth's magnetic field. As a result, the greatest modulation occurs at the equator and when the solar wind is most active (when solar flare activity is high). The flux resulting from the air shower is modulated by the density of the atmosphere (expressed as depth). Combining all of these factors results in the particle flux being a function of latitude, longitude, altitude and solar activity, with the greatest flux occurring at high altitudes over the poles during quiet periods of solar activity.

JEDEC Standard 89A, Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, (JESD89A) provides means for estimating neutron flux for a given latitude, longitude, altitude and level of solar activity, relative to a reference point set to the actual flux occurring at sea level in New York City.

JEDEC maintains a neutron flux calculator at www.seutest.com.

1.2 Packaging (Ask a Question)

Additional radiation sources can be found in packaging itself. Packaging materials used for integrated circuits contain trace amounts of uranium and thorium. These elements naturally emit alpha particles as they decay. Although alpha particles that result from decay have low penetration depth—a few centimeters of air can act as sufficient shielding—the proximity of packaging material to the silicon substrate make them an issue for electronic circuits.

For more details on the sources of ionizing radiation and its impact, see *Understanding the Impact of Single Event Effects on Programmable Logic*.

1.3 Dosage Rates for Networking Applications (Ask a Question)

Given the ubiquitous nature of the Internet and the interconnection networks used for System-on-Chip (SoC) devices, networking applications must function in a wide range of environments from sea level to mountainous terrain. While the neutron flux may be small at sea level, it generally increases with elevation and increasing latitude, so high altitude sites in high latitudes will experience the greatest flux. For example, the highest city in the world according to The Guinness Book of World Records is the city of Wenzhuan in China at 5,019 meters. At this location, the neutron flux is 20 times that of the reference location of New York City.

Table 1-1. Relative Neutron Flux at Selected Cities and Locations (from JESD89A)

Location	Latitude	Longitude	Elevation (m)	Atm. Depth(g/cm2)	Cutoff Rigidity (GV)	Relative Neutron Flux		
						Active Sun	Quiet Sun	Average
Cities								
Bangkok, Thailand	13.4°N	100.3°E	20	1031	17.4	0.51	0.53	0.52
Beijing, China	39.9°N	116.4°E	55	1027	9.4	0.71	0.76	0.73
Berlin, Germany	52.5°N	13.4°E	40	1028	2.8	0.94	1.08	1.01

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Location	Latitude	Longitude	Elevation (m)	Atm. Depth(g/cm2)	Cutoff Rigidity (GV)	Relative Neutron Flux		
						Active Sun	Quiet Sun	Average
Bogotá, Columbia	4.6°N	285.9°E	2586	753	12.3	3.7	4	3.85
Chicago, IL, USA	41.9°N	272.4°E	180	1011	1.8	1.09	1.28	1.19
Denver, CO, USA	39.7°N	255.0°E	1609	851	2.8	3.43	4.08	3.76
Hong Kong, China	22.3°N	114.2°E	30	1030	16.1	0.53	0.56	0.55
Houston, TX, USA	30.0°N	264.6°E	15	1031	4.6	0.88	0.98	0.93
Johannesburg, S. Africa	26.2°S	28.0°E	1770	834	7.1	2.95	3.3	3.13
La Paz, Bolivia	16.5°S	291.9°E	4070	623	12.2	8.59	9.39	8.99
London, UK	51.5°N	359.9°E	10	1032	2.9	0.91	1.05	0.98
Los Angeles, CA, USA	34.0°N	241.7°E	100	1021	5.3	0.89	0.99	0.94
Mexico City, Mexico	19.4°N	260.9°E	2240	787	8.4	3.75	4.16	3.96
Moscow, Russia	55.8°N	37.6°E	150	1015	2.2	1.06	1.22	1.14
New Delhi, India	28.6°N	77.2°E	220	1007	14.1	0.66	0.7	0.68
New York, NY, USA (ref)	40.7°N	286.0°E	0	1033	2.08	0.927	1.073	1
Paris, France	48.9°N	2.3°E	50	1027	3.6	0.92	1.04	0.98
Seattle, WA, USA	47.6°N	237.7°E	50	1027	2	0.97	1.13	1.05
Seoul, South Korea	37.6°N	127.0°E	50	1027	10.7	0.66	0.71	0.69
Sidney, Australia	33.9°S	151.2°E	30	1030	4.5	0.87	0.97	0.92
Singapore City, Singapore	1.3°N	103.9°E	15	1031	17.2	0.51	0.53	0.52
Stockholm, Sweden	59.3°N	18.1°E	30	1030	1.4	0.96	1.12	1.04
Taipei, Taiwan	25.0°N	121.5°E	10	1032	15.4	0.54	0.56	0.55
Toronto, Canada	43.7°N	280.6°E	120	1019	1.5	1.04	1.22	1.13
Tokyo, Japan	35.7°N	139.8°E	20	1031	11.6	0.62	0.66	0.64
Research Locations								
IAO, Hanle, Ladakh, India	32.8°N	79.0°E	4500	589	12.35	10.58	11.59	11.08
Jungfraujoch, Switzerland	46.5°N	8.0°E	3580	664	4.5	11.7	13.89	12.8
Leadville, CO, USA	39.25N	253.7°E	3100	706	3	9.74	11.85	10.79

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Location	Latitude	Longitude	Elevation (m)	Atm. Depth(g/cm2)	Cutoff Rigidity (GV)	Relative Neutron Flux		
						Active Sun	Quiet Sun	Average
Los Alamos Natl. Lab., USA	35.9°N	253.7°E	2250	786	3.9	5.15	6.06	5.6
Mauna Kea (CSO), HI, USA	19.8°N	204.5°E	4070	623	12.9	8.23	8.97	8.6
Mt. Fuji, Japan	35.4°N	138.7°E	3776	647	11.8	7.56	8.28	7.92
Plateau de Bure, France	44.6°N	5.9 E	2550	757	5.2	5.76	6.66	6.21
South Pole Station	90.0°S	—	2820	731	0.1	8.7	10.93	9.81
White Mtn. Res. Sta., USA	37.4°N	241.6°E	3810	644	4.2	13.72	16.41	15.07

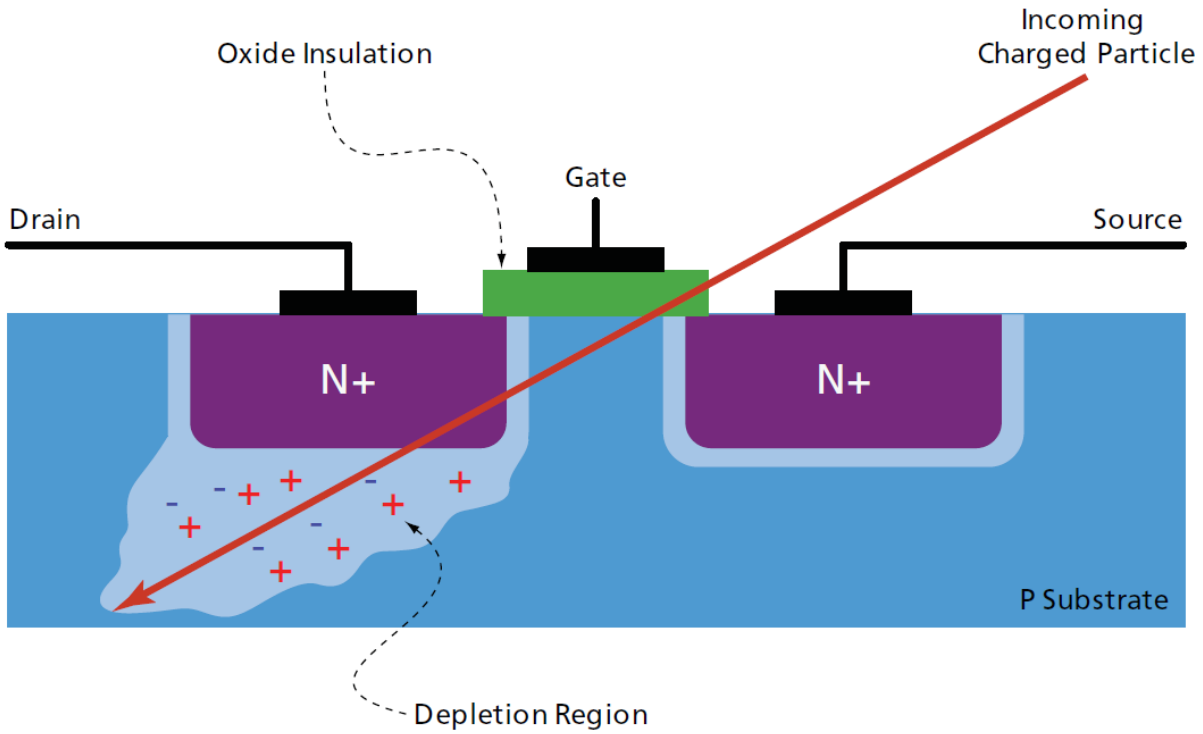
Granted, networking equipment is generally housed in concrete structures that attenuate the neutron flux. However, not all elements of the network benefit from this shielding. Often those elements located in areas of highest flux, such as mountain tops, are contained in thin-walled metal boxes, offering little shielding. Any network failure analysis must assume worst-case conditions.

2. Single Event Effects (Ask a Question)

Generally, any effect induced by a single radiation event on an electronic circuit (as opposed to effects due to collective dosage), whether transient or damaging, are collectively referred to as Single Event Effects (SEEs). There are three subclasses of SEEs that are the focus of this paper: Single Event Upsets (SEUs), Single Event Functional Interrupt (SEFIs), and Single Event Transients (SETs). For more details, see Understanding the Impact of Single Event Effects on Programmable Logic.

When charged particles strike the silicon substrate of an IC, they leave an ionization trail (see the following figure). Similarly, when a high-energy particle such as a neutron strikes the substrate, it collides with atoms in the substrate, liberating a shower of charged particles which then leave an ionization trail. For example, a neutron striking a silicon atom can release energy through elastic and inelastic scattering events or through spallation events that release magnesium and aluminum ions along with alpha particles and protons.

Figure 2-1. Impact of a High-Energy Particle



When a high-energy particle or ion impacts at the depletion region of an N-P junction, charges can collect in the region, creating voltage and current transients. The resulting charge can be sufficient to overpower the junction and cause a change in state (bit flip) of the memory element (SRAM cell, register, latch, or flip-flop). This change in state is referred to as a SEU. Because the effect is temporary, these errors are often referred as being soft—only the data stored in the element is corrupted.

Of special concern with respect to SEUs are SRAM-based FPGAs. The configuration memory of these devices is constructed out of SRAM cells. As a result, the configuration is susceptible to SEUs, possibly resulting in changing how the FPGA functions. In contrast, the configuration of antifuse and flash-based FPGAs is SEU-immune.

3. Assessing the Impact of SEEs (Ask a Question)

The following sections discuss and assess the impact of SEEs.

3.1 Assessing FIT Rates for SRAM-Based FPGAs (Ask a Question)

Determining potential Failures-in-Time (FIT) rates for a given SRAM-based FPGA is fairly straightforward (1 FIT = 1 failure/10^9 hours). The first step is to determine the relative neutron flux rate for the worst-case flight conditions (JESD89A references neutron flux relative to New York City). The relative flux rate can either be derived via the equations found in Annex A of JESD89A or determined via a web-based calculator based on the standard located at www.seutest.com/cgi-bin/FluxCalculator.cgi.

For example, for a router installed in a mountainous area such as Wenzhuan in China represents the near worst-case neutron flux for networking applications. Per JESD89A, that router experiences roughly 20 times the flux of the benchmark at New York City (during times of average solar activity).

The next step is to determine the per megabit upset rate for the configuration memory of the target FPGA. For Xilinx FPGAs, this information is published in the *UG116, Device Reliability Report*, published quarterly. The FIT rates published in this guide are derived from ongoing atmospheric testing on arrays of Xilinx FPGAs (as opposed to beam testing as specified by JESD89A). As such, this atmospheric testing includes upsets from all particles, not just from atmospheric neutrons and accounts for the shielding effect of the building. However; several studies have determined that the composition of GCR is fairly constant over altitude, allowing the relative neutron flux rate to be used as a scaling factor.

As an example, the worst-case FIT rate (at the 90% upper confidence band) per megabit for Kintex-7 FPGAs is 40.

The last data needed is the configuration memory size for the large FPGA. For Xilinx FPGAs, this data can be found in Xilinx UG470, *7 Series FPGAs Configuration User Guide*. For the 7K420T, the configuration memory size is listed at 149,880,032 bits or 149.88 MB.

The FIT rate calculation is shown in the following equation.

$$FIT = MemSize_{Config} \times ErrorRate_{Config} \times RelativeFlux_{Neutron}$$

For a Xilinx 7K420T operating in worst-case terrestrial environments, the resulting FIT rate is shown in the following equation.

149.88 MB x 40 FIT/Mb x 20 ≅ 119,000,000 FIT

This FIT rate translates to a Mean Time Between Failures (MTBF) of approximately one upset every 8403 hours or roughl one failure per year for a single device. Again, flash-based FPGAs are immune to configuration upset.

Note: MTBF (in hours) = 1billion/FIT

3.2 Assessing the Impact on the Network (Ask a Question)

Although assessing the total reliability is a complex task, arriving at a figure of merit for the potential impact of the FIT rate calculated above on a network can be done easily. In this estimation, only configuration upsets are considered. All other potential impacts such as memory upset, electrical noise and power outages are neglected.

Assume a network composed of ten complex routers, each built with ten 7K420Ts each for a total of 100 devices. The FIT from above must be multiplied by 100 to determine the FIT rate of the entire network, for a total network MTBF of one upset roughly every 84 hours or 104 upsets per year (see the following equation).

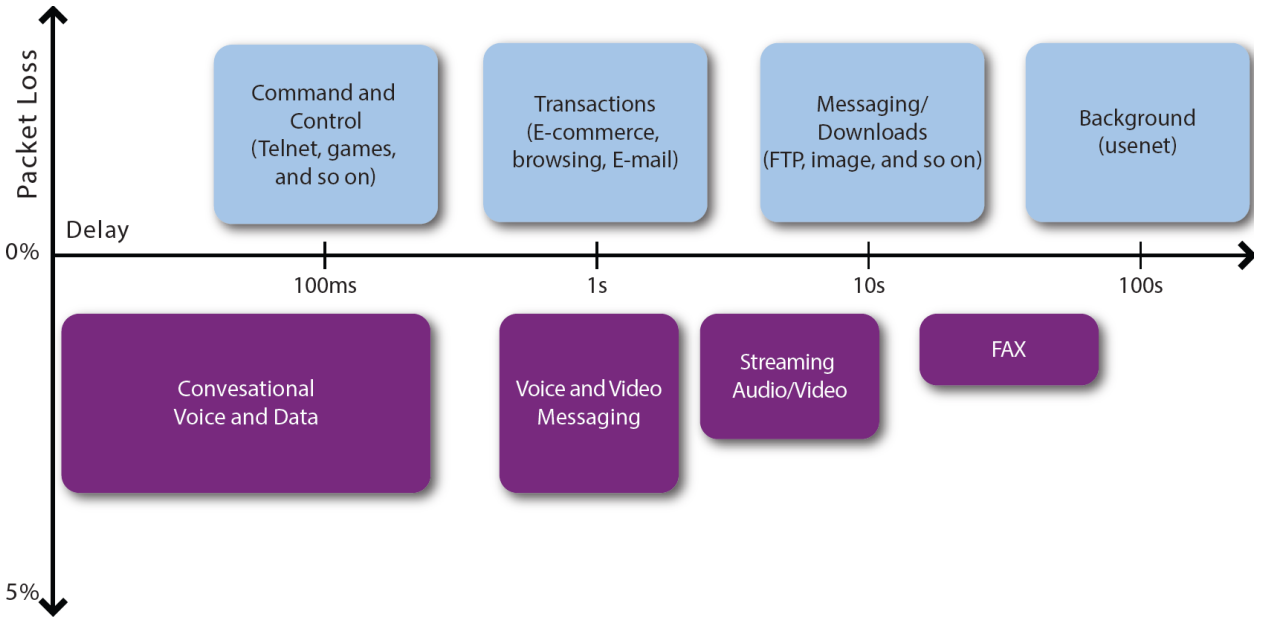
MTBF = 1B/(10 x 10 x 119,000,000 FIT) = 84 hours ≅ 104 upsets/yr

Converting from MTBF to system uptime is not straightforward because the length of time needed to recover from an error and reboot the system must be known. Assuming a router reboot time of one minute, the network above will suffer a downtime of 84 minutes or 99.98% availability before accounting for any other impacts to system reliability. Clearly addressing the issue of configuration memory upset is critical.

Note: For example, Cisco lists a cold reboot time of 2:03 minutes and a warm reload time of 21 seconds for the 7204 NPE 400 Router.

The following figure shows tolerance of various network application classes to delay and data loss. The size and shape of the boxes indicate the limit of delay and information loss tolerable for each application class. The applications above the horizontal line are tolerant to limited amounts of missing data, as indicated by the height of the box. Those falling below the 0% line will fail if any data is corrupt or missing. It is clear that the most challenging applications to run over a network are command-and-control applications; for example, network signalling traffic.

Figure 3-1. Sensitivity of Applications to Delay and Data Loss (After ITU-T G.1010)

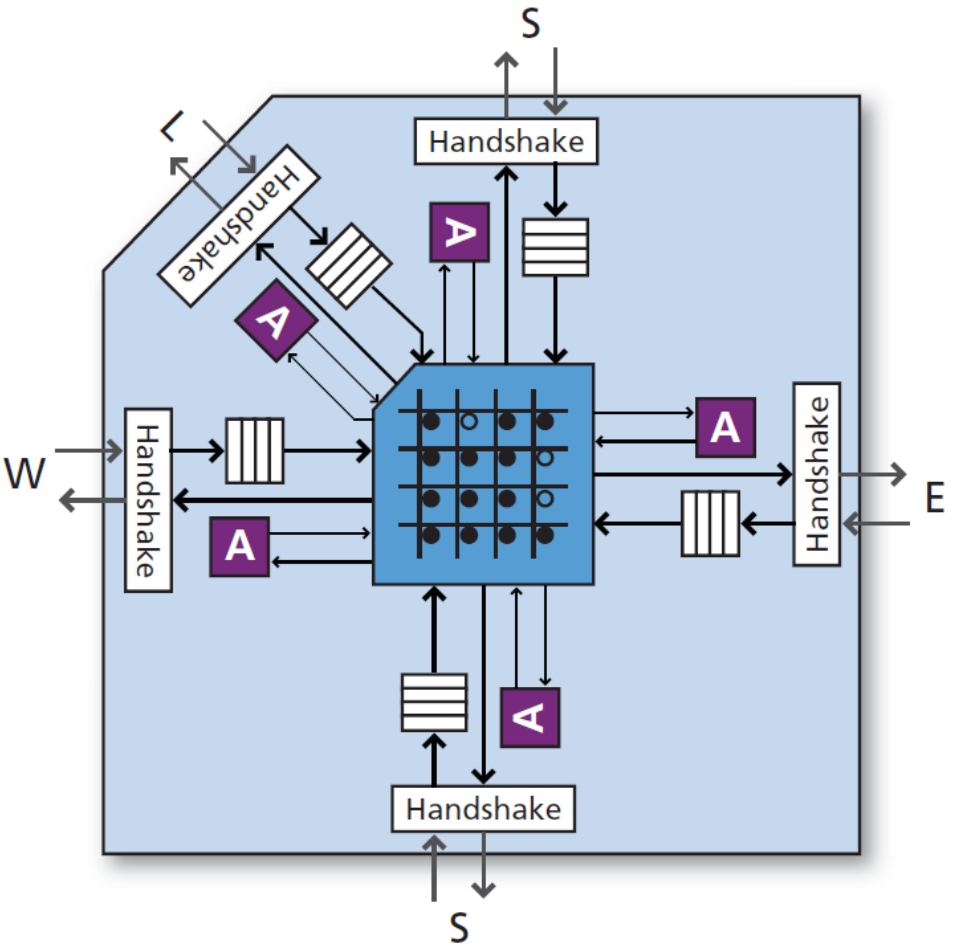


Network signaling traffic is the most important component of all network activity. For example, each time a device connects to the mobile network, signaling is used to start and end the network sessions regardless of the size and length of the session. The importance of signaling traffic is best described by the Signals Research Group report in January 2010, which found signaling traffic due to the increased use of smartphones to be the primary cause for increased congestion in 3G networks, reducing the quality of voice and data traffic and shortening battery life in mobile devices.

As shown in the preceding figure, signaling traffic requires a response time in the order of 100 ms and cannot tolerate any data loss. If these requirements are not met, command and control applications fail. This failure can be catastrophic, depending on the type of the application. In the event of an SEU, an SRAM-based FPGA consumes 25 ms to 100 ms just to detect an error, plus another 150 ms to 300 ms to do a soft reboot. It is quite clear that these delays are not acceptable for network signalling traffic because they are five times longer than the acceptable delay. Unlike SRAM-based FPGAs, Microchip's antifuse and flash-based FPGAs are immune to such SEUs.

The internet is not the only place where networks can be found. A network-on-chip (NoC) is an interconnection network that allows components in a system-on-chip (SoC) to communicate. The following figure provides an example router topology for NoCs, referred to as Router Architecture for SoC (RASoC).

Figure 3-2. General Architecture for the RASoC Router (After Frantz, et al)



A single router in this configuration uses 3,352 gates and 250 flip-flops. An NoC can have hundreds of routers or more, making the amount of memory used for buffering significant. Studies have shown that SEUs and SETs can have major effects on an NoC. These effects are of three categories, varying from routing errors to router crashes that can only be recovered by a hardware router reboot:

- Packet routing errors: These errors occur when an SEE alters the routing information in the packet header or the routing hardware in the router. This event causes packets to be improperly routed, never routed, or even overwritten inside the buffer.
- Payload errors: These errors are caused by SEEs in the router or an SEU that causes a bit flip in the payload word. These errors can change the payload length and the packet framing signals.
- Router crash: The most severe effect of SEEs on NoCs happens when a transient fault causes the router's state machine to go into an indefinite state from which it cannot recover, leading to a router crash. This effect is permanent and cannot be corrected by packet retransmission or any other software techniques. It can only be recovered after a hardware reset.

While some of these errors occur in the logic and memory of the circuit, an SEU in the configuration memory could result in similar errors. Automotive is another example where the influence of SEEs on an NoC is critical—modern vehicles host a general Electronic Computing Unit (ECU) interfaced with a collection of microelectronics systems to improve safety, efficiency, performance, entertainment, and comfort. The ECU can have a significant amount of on-board memories that are also susceptible to SEUs and SETs. Much of the ECU activities are safety-critical and have tight

deadlines; therefore, rebooting is not an option. As a result, these systems have almost no tolerance to SEUs and SETs and their reliability is critical—failure can be catastrophic.

Note: In 2007, the Automotive Electronics Council added a requirement for SEU testing for any device destined for an automotive application that contains more than 1 Mb of memory (AEC-Q100 Rev G).

3.3 Configuration Memory Mitigation (Ask a Question)

Because of the growing awareness of SEUs, manufactures of SRAM-based FPGAs recommend various mitigation techniques, ranging from simplistic to the more complex. The simplest method is to simply reconfigure the SRAM-based FPGA at regular intervals, clearing any SEUs that have accumulated. However, the time scale for reconfiguration is in the order of hundreds of milliseconds, during which, the function hosted in the FPGA is unavailable. This downtime is not acceptable in many networking applications.

With more recent generations of SRAM-based devices, the user can use the built-in error detection scheme in the configuration engine. Using a configuration memory readback feature, the CRC for each configuration frame is calculated and compared to a golden CRC. If a mismatch is detected, then an SEU has occurred, and the application can reconfigure the entire FPGA. Alternately, the application can attempt to correct the error and rewrite the frame in background.

Despite any correction, the errors still propagate, but the time before they are corrected is reduced when compared to periodic whole-device reconfiguration. Moreover, the detection time is still in the order of milliseconds, equating to millions of clock cycles before an upset can be corrected—certainly enough time for an error to propagate through even the most complex systems.

For more details on SEU mitigation techniques, see Understanding the Impact of Single-Event Effects on Programmable Logic.

3.4 Mitigation Does not Equal Immunity (Ask a Question)

Regardless of the methodology, mitigation is used to correct errors after the fact. In other words, it attempts to lessen their impact. In all cases, the correction schemes are only able to handle single-bit errors within a configuration memory frame. Any multi-bit errors require full device reconfiguration. In addition, mitigation schemes require additional reliability analysis and engineering time to implement and fully assess the impact of errors that still propagate. Mitigation should not be confused with immunity.

For more details on mitigation techniques, refer to *Understanding the Impact of Single-Event Effects on Programmable Logic*.

4. Summary (Ask a Question)

Various memory elements within electronic devices are suspectable to being upset when impacted by high-energy particles within the Earth's atmosphere. In addition, other elements of a device may propagate induced pulses or transients that can result in errors in function. In the critical functions of networking applications, these errors can cause a number of failures, including system crashes. Only one supplier of FPGAs offers devices whose base technology is fundamentally immune to upsets, helping suppliers of networking equipment achieve the five nines of system reliability. Building on a 20-year history of delivering high-reliability products to commercial avionics, military, and space applications, Microchip is uniquely positioned to help designers understand the impact of SEUs and SETs and mitigate their effect.

5. References (Ask a Question)

The following is a list of references:

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6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
Rev A	October 2023	This is the summary of changes in the revision A of the document: • Document was migrated to the Microchip template. • Document number was updated from 55900138 to DS50003592A. • Updated the 3.1. Assessing FIT Rates for SRAM-Based FPGAs section. • Updated the 3.2. Assessing the Impact on the Network section.

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