Understanding the Impact of Single Event Effects in Avionics Applications

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Overview

With modern, long-haul passenger aircrafts operating at altitudes near 40,000 feet on polar flight paths, both the passengers and the aircraft electronics are subjected to high levels of ionizing radiation. In addition to affecting the long-term health of passengers, this radiation can impact the function of and data stored in avionics systems. While the impact of this radiation on memory circuits in avionics has been known since 1992, its impact on programmable logic is not widely understood by the engineering community—nor is it widely known that not all FPGA technologies share the same risks. With DO-254's focus on safety, it is incumbent on avionics designers to quantify these risks and understand how differing FPGA technologies react in this environment.

Sources and Effects of Ionizing Radiation

Galactic Cosmic Rays

Galactic cosmic rays (GCR), comprised of high-energy particles, overwhelmingly protons, impact the Earth's atmosphere constantly. These particles, originating in space, have sufficient energy to liberate nuclei when they collide with molecules in the Earth's atmosphere. The result of this collision is referred to as an air shower, where a wide range (and high number) of particles are generated. The primary spallation products of concern to avionics designers are neutrons and protons (in addition to remanent cosmic rays).

The flux of cosmic rays impacting the Earth's atmosphere is modulated by both the solar wind and the Earth's magnetic field. As a result, the greatest modulation occurs at the equator and when the solar wind is most active, which is when solar flare activity is high. The flux resulting from the air shower is modulated by the density of the atmosphere (expressed as depth). Combining all of these factors results in the particle flux being a function of latitude, longitude, altitude and solar activity, with the greatest flux occurring at high altitudes over the poles during quiet periods of solar activity.

As a result, an observer in an aircraft flying at 40,000 feet over the poles during a period of moderate solar activity experiences more than 500 times the neutron flux as a terrestrial observer in New York City.

Packaging

Additional radiation sources can be found in packaging itself. Packaging materials used for integrated circuits contain trace amounts of uranium and thorium. These elements naturally emit alpha particles as they decay. Although alpha particles that result from decay have low penetration depth—a few centimeters of air can act as sufficient shielding—the proximity of packaging material to the silicon substrate makes them an issue for electronic circuits.

For more details on the sources of ionizing radiation and its impact, see the *Understanding Single Event Effects in FPGAs* white paper.

Dosage Rates for Commercial Avionics

In addition to the flux of high-energy particles, there is also concern about the total ionizing dose (TID) a device receives over its operation life and the possible impact on device performance. Since air crew are exposed to the same dosage as the electronics, an estimate of electron device lifetime exposure can be approximated based on crew exposure data.

Given that the maximum dosages are on long-haul flights (see Table 1) and assuming that the aircraft receives twice the dosage as the air crew (one crew to Tokyo, a second crew for the return to New York) and a maximum of one round trip per day, the yearly total dose for the Tokyo-New York aircraft is shown in EQ 1:

$$2 \times 75.4\ \mu Sv \times 365 \cong 55\ mSv$$

EQ 1

Assuming a 20-year life for an avionics system, the maximum total dose received would be on the order of 1.1 Sv or approximately 110 Rad. Since TID effects are not seen in electronic devices until tens of Krad, the cumulative impact of ionizing radiation on avionics is not of concern.

Table 1: **Calculated Effective Dose of Galactic Cosmic Radiation Received on Air Carrier Flights**

Origin – Destination	Maximum Altitude (thousands of feet)	Air Time (hours)	Total Dose (µSV)
New York NY – Tokyo JP	43	13.0	75.4
Tokyo JP – New York NY	41	12.2	69.6
London UK – Los Angeles CA	39	10.5	61.6
Athens GR – New York NY	41	9.4	61.3
London UK – Chicago IL	39	7.8	47.5
London UK – Dallas / Ft. Worth TX	39	9.7	43.7
Los Angeles CA –- Tokyo JP	40	11.7	43.4
Chicago IL – London UK	37	7.3	43.0
Dallas / Ft. Worth TX – London UK	37	8.5	39.6
London UK – New York NY	37	6.8	37.4
Tokyo JP – Los Angeles CA	37	8.8	33.4
Lisbon PG – New York NY	39	6.5	28.9
New York NY – Seattle WA	39	4.9	28.0
San Francisco CA – Chicago IL	41	3.8	20.7
Chicago IL – San Francisco CA	39	3.8	19.4
Seattle WA – Washington DC	37	4.1	19.2
Washington DC – Los Angeles CA	35	4.7	19.1
Seattle WA – Anchorage AK	35	3.4	16.9
Honolulu HI – Los Angeles CA	40	5.1	16.4
Los Angeles CA – Honolulu HI	35	5.2	14.7
New York NY – San Juan PR	37	3.0	10.1
New York NY – Chicago IL	39	1.8	8.92
Tampa FL – St. Louis MO	31	2.0	4.71

Table 1: **Calculated Effective Dose of Galactic Cosmic Radiation Received on Air Carrier Flights (continued)**

Origin – Destination	Maximum Altitude (thousands of feet)	Air Time (hours)	Total Dose (μSV)
New Orleans LA – San Antonio TX	39	1.2	3.27
St. Louis MO – Tulsa OK	35	0.9	1.71
Miami FL – Tampa FL	24	0.6	0.39
Seattle WA – Portland OR	21	0.4	0.17
Houston TX – Austin TX	20	0.5	0.17

Note: *Adapted from* What Aircrews Should Know About Their Occupational Exposure to Ionizing Radiation.

Single Event Effects

Generally, any effect induced by a single radiation event on an electronic circuit (as opposed to effects due to collective dosage), whether transient or damaging, are collectively referred to as single event effects (SEEs). There are three subclasses of SEEs that are the focus of this paper: single event upsets (SEUs), single event functional interrupt (SEFIs), and single event transients (SETs). See the *Understanding Single Event Effects in FPGAs* white paper for more details.

When charged particles strike the silicon substrate of an integrated curcuit (IC), they leave an ionization trail (Figure 1). Similarly, when a high-energy particle, for example a neutron, strikes the substrate, it collides with atoms in the substrate, liberating a shower of charged particles, which then leave an ionization trail. For example, a neutron striking a silicon atom can release energy through elastic and inelastic scattering events or via spallation events that release magnesium and aluminum ions along with alpha particles and protons.

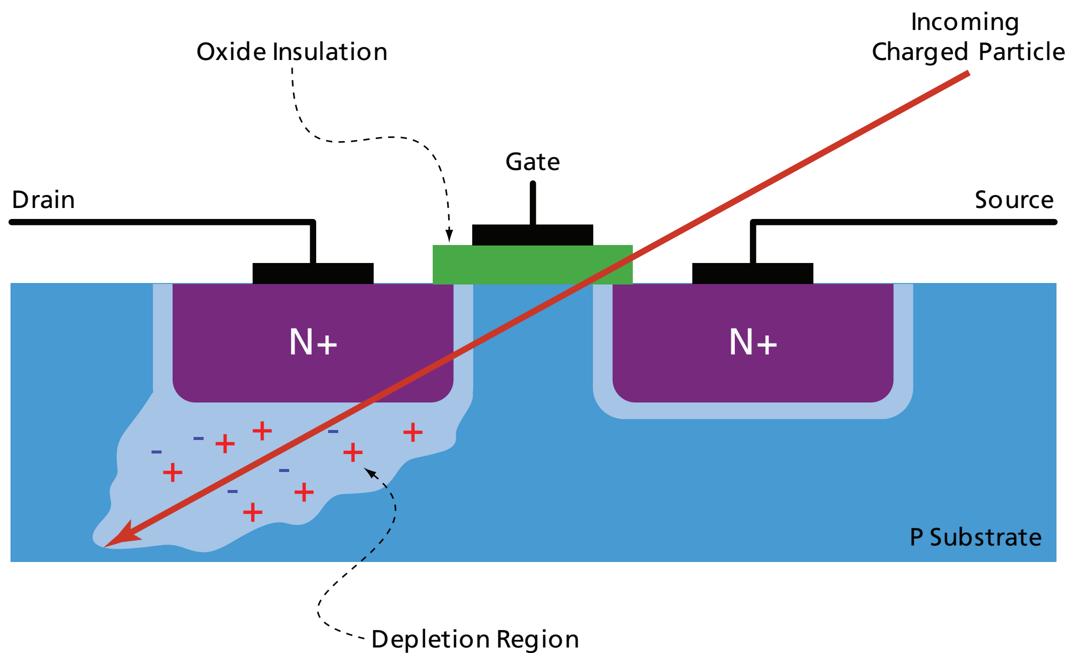

Figure 1: **Impact of a High-Energy Particle**

When a high-energy particle or ion impacts at the depletion region of a N-P junction, charges can collect in the region, creating voltage and current transients. The resulting charge can be sufficient to overpower the junction and cause a change in state (bit flip) of the memory element (SRAM cell, register, latch, or flip-flop). This change in state is referred to as an SEU. Because the effect is temporary, these errors are often referred as being soft—only the data stored in the element is corrupted.

Of special concern with respect to SEUs are SRAM-based FPGAs. The configuration memory of these devices is constructed from SRAM cells. As a result, the configuration is susceptible to SEUs, possibly resulting in changing how the FPGA functions. In contrast, the configuration of antifuse and flash-based FPGAs is SEU-immune.

Assessing the Impact of SEEs

DO-254 and SEEs

Anyone designing flight hardware has to be concerned with DO-254 certification. DO-254, *Design Assurance Guidance for Airborne Electronic Hardware*, defines a framework for design assurance and certification for airborne electronic hardware (AEH) to ensure safe operation.

As a part of the design process, the standard requires that a hardware safety assessment (Section 2.3) must be performed. This assessment determines the criticality (design assurance level) for each functional block in the system and must identify potential functional failure paths (FFPs). For SRAM-base FPGAs, GCR-induced SEEs are considered as potential FFPs and require that an assessment be made of the risk of SEEs and a mitigation plan be developed.

Assessing FIT Rates for SRAM-based FPGAs

Determining potential failures-in-time (FIT) rates for a given SRAM-based FPGA is fairly straightforward (1 FIT = 1 failure/10^9 hours). The first step is to determine the relative neutron flux rate for the worst-case flight conditions (JESD89A references neutron flux relative to New York City). The relative flux rate can either be derived via the equations found in Annex A of JESD89A or determined via a web-based calculator based on the standard located at www.seutest.com/cgi-bin/FluxCalculator.cgi.

For example, an aircraft traveling on a long-haul route near the poles at 40,000 feet will experience the worst-case neutron flux for commercial flight. Per JESD89A, that aircraft will experience 561.7 times the flux at the benchmark in New York City (during times of average solar activity).

The next step is to determine the per megabit upset rate for the configuration memory of the target FPGA. For Xilinx FPGAs, this information is given in UG116, *Device Reliability Report*, published quarterly. The FIT rates published in this guide are derived from ongoing atmospheric test on arrays of Xilinx FPGAs (as opposed to beam testing as specified by JESD89A). As such, this atmospheric testing includes upsets from all particles, not just from atmospheric neutrons. However; several studies have determined that the composition of GCR is fairly constant over altitude, allowing the relative neutron flux rate to be used as a scaling factor.

As an example, the worst-case FIT rate (at the 90% upper confidence band) per megabit for Virtex®-5 FPGAs is 186.3.

The last data needed is the configuration memory size for the large FPGA. For Xilinx FPGAs, this data can be found in Xilinx XAPP1073, *NSEU Mitigation in Avionics Applications*. For the XC5VLX110T, the configuration memory size is listed at 31,118,848 bits or 29.68 Mb.

The FIT rate calculation is shown in EQ 2.

$$FIT = MemSize_{Config} \times ErrorRate_{Config} \times RelativeFlux_{Neutron}$$

EQ 2

For a Xilinx XC5VLX110T operating at 40,000 feet near the poles, the resulting FIT rate is shown in EQ 3.

$$29.68\ Mb \times \frac{186.3\ FIT}{Mb} \times 561.7 \cong 3{,}105{,}858\ FIT$$

EQ 3

This FIT rate translates to a mean time between failures (MTBF) of approximately one upset every seven weeks. But this rate is for a single device. If an airframe made extensive use of this FPGA, for example, with four to five of this FPGA per line replaceable unit (LRU) and assuming 20 LRUs total in the airframe, then this aircraft would experience an upset every 3.5 hours. Unlike SRAM-based FPGAs, antifuse and flash-based FPGAs are immune to configuration upset.

Configuration Memory Mitigation

Because of the growing awareness of SEUs, manufacturers of SRAM-based FPGAs recommend various mitigation techniques, ranging from simplistic to the more complex. The simplest method is to reconfigure the SRAM-based FPGA at regular intervals, clearing any SEUs that have accumulated. However, the time scale for reconfiguration is on the order of hundreds of milliseconds, during which the function hosted in the FPGA is unavailable. This downtime may not be acceptable in many applications.

With more recent generations of SRAM-based devices, the user can employ the built-in error detection scheme in the configuration engine. Using a configuration memory readback feature, the CRC for each configuration frame is calculated and compared to a golden CRC. If a mismatch is detected, then an SEU has occurred, and the application can reconfigure the entire FPGA. Alternately, the application can attempt to correct the error and rewrite the frame in background.

Despite any correction, the errors still propagate. Only the time before they are corrected is reduced when compared to periodic whole-device reconfiguration. Moreover, the detection time is still on the order of milliseconds, equating to millions of clock cycles before an upset can be corrected—certainly enough time for an error to propagate through even the most complex systems.

For more details on SEU mitigation techniques, see the *Understanding Single Event Effects in FPGAs* white paper.

Mitigation Does Not Equal Immunity

Regardless of the methodology, mitigation is used to correct errors *after* the fact. In other words, it attempts to *lessen* their impact. In all cases, the correction schemes are only able to handle single-bit errors within a configuration memory frame. Any multi-bit errors require full device reconfiguration. In addition, mitigation schemes require additional reliability analysis and engineering time to implement and fully assess the impact of errors that still propagate. Mitigation should not be confused with immunity.

Summary

Various memory elements within electronic devices are suspectable to being upset when impacted by high-energy particles within the Earth's atmosphere. In addition, other elements of a device may propagate induced pulses or transients that can result in errors in function. Given the high neutron flux found at commercial altitudes, avionics designers must consider the impact of SEUs.

Only one supplier of FPGAs offers devices with a base technology that is fundamentally immune to upset. Building on a 20-year history of delivering high-reliability products to commercial avionics, military, and space applications, Microsemi is uniquely positioned to help designers understand the impact of SEUs and SETs and mitigate their effect.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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